論文

# 半導体技術を用いて作製した薄膜キャパシタの実装方法の検討

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## A Study on the Method to Embed the Thin Film Capacitor Fabricated by Semiconductor Technology

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**Abstract**

Recently embedded passive devices have been actively investigated in an effort to save the surface area on printed circuit boards. About 60% of the area is occupied by the passive parts. As suggested in the previous paper, thin-film capacitors prepared using a semiconductor technology are one of the most promising candidates. In this paper, these film capacitors were embedded using two different methods. One was a conventional method using solder bump, and the other was a newly-developed method using conductive paste. The solder bump was formed using screen-printing following the wafer-level chip-size package (W-CSP) process. Since the solder bump is currently in practical use, high reliability should be expected. However, the chips formed by this method became thicker due to copper posts, solder bumps, and so on. The other method, using conductive paste, has the advantage of connection without any thickness problem. After embedding and solder heat tests, the capacitance of all the chips did not change, and the differences between before and after the tests are within the acceptable margin of error. However, in most cases, the loss (tan $\delta$) increased slightly after the embedding and solder heat tests. In only one case did the solder heat test for an embedded BST capacitor chip connected by conductive paste show a lower tan $\delta$ value than that in the previous test. Based on all the results, the two methods used in this study are concluded to have a high potential for use in embedding methods. Further reliability tests are necessary for practical use.

***Key Words***: *Embedded Passive, Thin Film Capacitor, Semiconductor Process*