「エレクトロニクス実装学会誌」6〔4〕326~331 (2003)

論文

SiP (System in Package) の電気特性評価

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Electrical Characteristic of SiP (System in Package)

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Abstract

We performed the transmission line simulation when changing four kinds of package structures in the same chip combination. And two kinds of SiPs were actually produced among those, and the setup time was measured. The following results were obtained: (1) We have checked that Signal Integrity deteriorated, so that wiring length became long. (2) We checked the crosstalk noise in the flip-wire type with which parallel wiring length becomes long. The noise was a satisfactory level although it generated. (3) We calculated the setup margin with each package structure. The difference is about 0.1 nsec at the maximum. (4) We surveyed the wire-wire type and flip-wire type setup time. Both differences were about 0.4 nsec at the maximum.

Key Words: *SoC, SiP, Signal Integrity, Interposer, Transmission Line Simulation*