●技術報告



# 表面張力を利用したSi薄ダイのセルフアライメントにおけるロバスト性評価

廣島　満*，有田　潔*，土師　宏*，Christof LANDESBERGER**，Karlheinz BOCK**

## A Robustness Study on Self-Alignment of Thin-Si Dies Using Surface Tension

Mitsuru HIROSHIMA*, Kiyoshi ARITA*, Hiroshi HAJI*, Christof LANDESBERGER**, and Karlheinz BOCK**

* パナソニックファクトリーソリューションズ（株）（〒571-8502 大阪府門真市松葉町2番7号）
** Fraunhofer Research Institution for Modular Solid State Technologies EMFT (Hansastrasse 27 d, 80686 Munich, Germany)
* Panasonic Factory Solutions Co., Ltd. (Matsuba-cho 2-7, Kadoma, Osaka 571-8502, Japan)
** Fraunhofer Research Institution for Modular Solid State Technologies EMFT (Hansastrasse 27 d, 80686 Munich, Germany)

**Abstract**

We found that self-alignment accuracy was better than ±2 μm in the case with an initial offset of up to 1 mm. This method, driven by the surface tension force of the liquid, offers new technical solutions for both high accuracy chip bonding and low cost placement manner. Some important points, such as wetting behaviour, die release offset, and the influence of defects on a die, were studied in order to suggest approaches to robustness in this new technique.

***Key Words*:** *Self-Alignment, Chip on Wafer, Thin-Si Die, Surface Tension*