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高い2次実装信頼性を有する樹脂応力緩和層型ウエハレベルチップサイズパッケージの開発

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Development of Resin Stress Buffer Layer Type Wafer Level Chip Size Package with High Reliability for Board Level Test

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Abstract

Remarkable progress has been made in the development of electronic devices, especially in portable applications. This field requires packaging technologies that allow for smaller structures with higher density. To satisfy this demand, a W-CSP (Wafer-level Chip Size Package) with a resin stress buffer layer has been developed. The incredibly small package size and simple structure of the W-CSP creates an important issue: how to decrease thermal mechanical stress caused by differences in the coefficient of thermal expansion between the IC chip and the daughter substrate. In this paper, we describe the development of a W-CSP structure that includes a resin stress buffer layer with high thermal cycle reliability for BLTs (Board Level Tests), using thermal mechanical analysis and a novel W-CSP structure with two redistribution circuit layers. The lifetime of this novel structure is twice as long as that of an ordinary W-CSP for a thermal cycle BLT.

Key Words: *Wafer Level Package, Design, Reliability, Simulation, Board Level Test*