April 19

	Room A	Room B
10:00 12:05	WA1: MEMS & Optoelectronics 1. Micro-mirror Array Fabricated Using Magnetic Alignment T. Uemura, Tokyo Metropolitan University / Japan 2. Ceramic Wafer Scale Packaging Technology for MEMS Devices I. Ishii, F. Itou, T. Maeda, K. Makinouchi, K. Yoshida, K. Tagami, T. Hirakawa, K. Onitsuka, Kyocera / Japan 3. STP Technology for MEMS Devices Packaging N. Sato, K. Kuwabara, T. Sakata, H. Ishii, NTT, K. Tamei, K. Kudou, NTT Advanced Technology, K. Machida, NTT / Japan 4. Self-Written Waveguide Optical Pin Fabricated Using Photomask-transfer Method H. Hanajima, Y. Obata, H. Ozawa, O. Mikami, T. Uchida, Tokai University / Japan 5. Optical Connection Rod on VCSEL Using Self-Written Waveguide by Mask-transfer Process M. Kanda, Y. Obata, H. Kubo, O. Mikami, Tokai University / Japan	WB1: Interconnection 1. **Yield Based Manufacturing Cost Methodology for Advanced Packaging Technology Comparison** (Session Invited) C. E. Bauer, H. J. Neuhaus, TechLead / USA 2. Correct Reflow Machine Makes Your Process More Robust J. Lempinen, A. Tuominen, University of Turku / Finland 3. The Chip-on-Glass Bonding Using Non-conductive Adhesive and Sn Bump; Effect of Sn Bump and Pad Types S. M. Lee, B. Y. Kim, Y.-H. Kim, Hanyang University / Korea 4. Formation of Kirkendall Voids in the Reactive Diffusion between Cu and High Lead Solders S. Ishikawa, Kumamoto University / Japan 5. Characteristics of Bonding Process Using Ag Metallo-Organic Nanoparticles A. Hirose, Osaka University / Japan
	Lunch Time	
13:35 13:45	Welcome Speech I. Kaneko (ICEP 2006 General Chairperson, Musashi Institute of Technology)	
13:50 14:00	Awarding Ceremony ICEP 2005 Best Papers IEEE CPMT Young Award	
14:05 15:25	Focused Seminar: SiP Progress in Japan and USA 1. Portable Electronic Products Driven by SiP and High-dense Module Technologies H. Ueda, SemiConsult / Japan 2. The New Markets for SiP E. J. Vardaman ,TechSearch International / USA	
15:35 17:35	Invited Speech 1. **What's the Jisso Technology for Next Generation Automotive Electronics** Dr. Masayuki Hattori, Toyota Motor Corporation 2. **Advanced Semiconductor Packaging Technology** Dr. Jungihl Kim, Amkor Technology Korea, Inc.	
18:00 20:00	Welcome Reception Shinagawa Prince Hotel (New Tower)	

April 20

	Room A	Room B
9:00	TA1:Embedded Technology	TB1:Materials
	1. **Embedded Chip Build-Up BGA for High-End Processors** (Session Invited) R. A. Fillion, GE Global Research, C. E. Bauer, TechLead, C. G. Woychik, J. Erlbaum, GE Global Research / USA 2. Embedded Capacitor Technology on FR-4 Using Aerosol Deposition Y. Imanaka, N. Hayashi, M. Takenouchi, Fujitsu, J. Akedo, National Institute of Advanced Industrial Science and Technology / Japan 3. Preparation and Evaluation of Embedded Passive Thin Film Capacitor by Using Semiconductor Technology M. Watanabe, I. Koiwa, H. Honma, Kanto Gakuin University, K. Ashikaga, M. Terui, Y. Shiraishi, N. Anzai, T. Ohsumi, Oki Electric Industry, T. Osaka, Waseda University, T. Kumagai, Y. Sato, Tokyo Ohka Kogyo, A. Hashimoto, Kanto Gakuin University / Japan 4. Process Development and Surface Characterization on Liquid Crystalline Polymer Substrate Based System on Package with Chip Embedded for Electronic Application Q. Zhang, Shanghai University, Chalmers University of Technology, Z. Lai, U. Jelvestam, G. Fritze, Chalmers University of Technology, Z. Cheng, Shanghai University, L. Nyborg, Chalmers University of Technology, J. Liu, Shanghai University, Chalmers University of Technology / Sweden	1. New Developed Solvent-Casting Type LCP Film Suitable for PCB Applications T. Ito, Sumitomo Chemical / Japan 2. Repairable Underfill which Yield Plastic Flow before Cure K. Kawate, Sumitomo 3M / Japan 3. Filler Size Effect of Underfill in Flip-chip Package W. S. Lee, Hynix Semiconductor / Korea 4. Thermal Characteristic and Morphology of Conductive Polymer Poly(9.9'-dioctylfluorene-co-bithiophene) Film D.-J. Tsai, C.-L. Chung, G.-J. Chen, S.-L. Fu, I-Shou University / Taiwan
10:40		
10:50	5. **Embedding Discrete Components into Organic Substrates** (Session Invited) R. Tuominen, Imbera Electronics Oy / Finland 6. Development of Embedded Organic Module Technology M. Miyazaki, Taiyo Yuden / Japan 7. Thin Film Embedded Passive Technology for System Integration S. Kuramochi, T. Mori, K. Suzuki. Dai Nippon Printing, Y. Fukuoka, Worldwide Electronic Integrated Substrate Technology Inc / Japan 8. Development of the Embedded Passive Substrate and High Frequency Characteristics S. Utsumi, Mitsubishi Electric / Japan	TB2: Reliability 1. Paradigm Shift for PWB Surface Finishes in Mobile Phone Terminals C. W. Nielsen, Nokia Mobile Phones / Denmark 2. Estimate to Drop Impact Reliability for BGA Solder Joints H. Nishiuchi, T. Sogo, Toshiba / Japan 3. Open Lead Detection Based on Supply Current of CMOS Logic Circuits by AC Voltage Signal Application M. Hashizume, The University of Tokushima / Japan 4. Reliability of Gold-Solder Bump Joint J.-Y. Kim, Y. B. Sun, Kyonggi University / Korea
12:30		
	Lunch Time	
14:00	TA3: Solution for High Frequency & High Performance	TB3: Simulation
	1. **On-chip/Off-chip High Density Transmission Line Interconnect** (Session Invited) K. Masu, Tokyo Institute of Technology / Japan 2. Enhanced Packaged Transistor Modelling for 24GHz LTCC Applications V. Napijalo, V. Cojocaru, TDK Electronics Ireland, T. Yokoyama, TDK, T. Young, TDK Electronics Ireland / Ireland, Japan 3. RF Benchmarking of LTCC Circuits up to 40GHz D. E. J. Humphrey, B. Verner, V. Cojocaru, B. Clarke, T. Young, V. Napijalo, TDK Electronics Ireland / Ireland 4. Dielectric Constant Analysis of Low Temperature Co-fired Ceramic Substrates in GHz Range W. Choi, Fukuoka Industry, Science and Technology Foundation, T. Kawamura, H. Tomokage, Fukuoka University / Japan	1. Viscoelastic FEM Simulation of an Underfill Resin for the Reliability Evaluation of Solder Bumps in a Flip Chip Package T. Kondo, NEC / Japan 2. Thermal Resistance Analysis on Semiconductor Packages Using Two Mesh Models H. Sueyoshi, Fukuoka University, I. Ohkubo, Saga Electronics, W. Choi, Fukuoka Industry, Science & Technology Foundation, S. Yoshida, New Japan Radio, H. Tomokage, Fukuoka University / Japan 3. Implementation of Bulk Driven OTAs in Second Order Lowpass Filter M. B. Zainal, Kolej University Teknologi Tun Hussein Onn / Malaysia 4. Study of Impact Stress of CSP Solder Joints Using Homogenization Method and FEM Drop-Simulation I. Hirata, NEC, H. Nakamura, NEC TOPPAN CIRCUIT SOLUTIONS / Japan
15:40		
15:50	5. The Development of Surface Mount Package with Differential Transmission Lines for 40Gb/s Applications K. Kawabata, K. Tagami, T. Kubo, Kyocera / Japan 6. On the Local Skew Effect on the Electrical Performance of Differential Via Structures in a Multilayer PCB T. Kushta, Y. Wakabayashi, T. Harada, NEC, T. Kaneko, S. Nakamura, NEC Electronics / Japan 7. A Vertical Transition for Packaged Transistors on LTCC Substrates for 24Ghz Applications V. Napijalo, B. Kearns, TDK Electronics Ireland / Ireland 8. A Study on Magnetic Field Measurements by a High-Frequency-Carrier Type Magnetic Probe Y. Kayano, Akita University, K. Tan, K. Yamakawa, T. Komakine, Akita Research Institute of Advanced Technology, H. Inoue, Akita University / Japan	TB4:PoP/SiP 1. Ultimate Super Chip Integration T. Fukushima, Y. Yamada, H. Kikuchi, T. Tanaka, M. KOyanagi, Tohoku University / Japan 2. Electrical Signal Integrity between DSP and Memory in 3D Packages for Mobile Phones K. Takao, C. Azuma, M. Amagai, Texas Instruments, Japan / Japan 3. A Study of Package Flatness during Solder Reflow for Package-on-Package(POP) Y. Suzuki, K. Abe, E. Yamada, M. Amagai, Texas Instruments, Japan / Japan 4. LC-VCO with Wafer Level CSP Technology S. Takagi, Seiko Epson / Japan
17:30		

April 21

	Room A	Room B
8:50	FA1: Si Through Hole Technology	(9:40)
	1. **Silicon Through Hole Technology** (Session Invited) S. Denda, Nagano Prefectural Institute of Technology / Japan (40 minutes) 2. Impact and Opportunities of Through Silicon Via and Three-Dimensional Chip Stacking K. Takahashi, Toshiba / Japan (9:55-10:05 Break) 3. Room Temperature Bonding between Stacked Chips Formed Si Through-hole Electrodes N. Tanaka, Y. Yoshimura, T. Naito, T. Akazawa, Hitachi / Japan 4. Through-hole Interconnection Technologies in Si Substrate for Wafer Level Package T. Takizawa, Fujikura / Japan 5. Silicon Through Interconnection Technology for System Integration D. Kitayama, S. Chujyo, T. Maruyama, M. Akazawa, T. Takano, K. Nakayama, M. Yamaguchi, H. Mawatari, S. Kuramochi, K. Suzuki, Dai Nippon Printing, Y. Fukuoka, Worldwide Electronic Integrated Substrate Technology Inc / Japan	--- FB1: Lead Free 1. **Impact Reliabilities of Lead-free Solder Joints with Cu, Ni, and Ni(P) Metallizations** (Session Invited) J. Yu, Y. C. Sohn, J. Y. Kim, Y. K. Jee, Y. H. Ko, KAIST / Korea 2. Intermetallic Compound Formation between Sn and Cu or Ni T. Sasaki, M. Tanaka, Nippon Steel, Y. Ohno, Kumamoto University / Japan 3. Application Characteristics and Interface Structure of Lead-Free Low Temperature Sn-Zn Solder Material G. Chen, Tsinghua University, J. Tang, National Institute for Materials Science, Y. Liu, J. Ma, Tsinghua University / China, Japan 4. Reliability of Sn/Pb, Sn/Pb/Ag, Sn/Ag/Cu and Sn/Cu/Ni Solder Joints in Cyclic Mechanical Loading J. Lempinen, A. Tuominen, T. Kerminen, I. Tuokko, University of Turku / Finland
11:20		
11:30	FA2: Latest JISSO Application	5. Investigation of Whisker Formation on Tin Plating H. Yasuda, Y. Harasaki, Y. Watanabe, K. Tokio, R. Kimizuka, Ebara Udylite / Japan 6. Consequential Toxicity Assessment of the Global Shift to Pb-free Solder Paste A. S. G. Andrae, SMIT, Chalmers University of Technology, J. Liu, SMIT, Chalmers University of Technology, Shanghai University / Sweden, China
	1. Analysis of Corrective Actions Quality Provided to Customers with Mobile Terminals A. Mwegerano, P. Kytosaho, Nokia, A. Tuominen, University of Turku / Finland 2. Is the Productization of a Mobile Terminal Coming More Demanding? T. Rantala, Nokia, A. Tuominen, University of Turku / Finland	
12:20		
	Lunch Time	
13:50	FA3: Recent Progress of the Surface Activated Bonding Technology in Electronic Packaging	FB3: Substrate & Interposer, Practical/Profittable Approach
	1. **Current Status and Future Outlook of SAB Technology** (Session Invited) T. Suga, The University of Tokyo / Japan 2. Bumpless Interconnect of Cu Electrodes in Millions-Pins Level A. Shigetou, T. Itoh, T.Suga, The Unversity of Tokyo / Japan 3. Low Temperature Surface Activated Flip Chip Technique on Cu-Cu Interconnection of Chip-On-Flex System Z. Xu, T. Suga, The University of Tokyo / Japan 4. Low Temperature Bonding of Sn-Ag-Cu Solder Bumps by SAB Method W. Yinghui, X. Zhonghua, T. Suga, The University of Tokyo / Japan	1. Halogen Free Material Having Low Transmission Loss Designed for Multi-layer Printed Circuit Board Applications H. Inoue, Matsushita Electric Works / Japan 2. The Indistinct Approach to an Estimation of Condition of Film Resistors and Hybrid Integrated Circuits Y. Antonov, L. Zade, Ulyanovsk State Technical University / Russia 3. Development of a High-density Multilayer Flexible Printed Circuit Board H. Satoh, Sumitomo 3M / Japan 4. In Situ Charge Observation in Insulation Layers of Printed Circuit Boards during Ageing Tests K. Fukunaga, NICT, K. Okamoto, Fuji Electric Advanced Technology / Japan 5. Development of Halogen-free Prepreg Available for Additive Manufacturing Process S. Araki, Matsushita Electric Works / Japan
	(15:30 - 15:40 Break)	(15:55 - 16:05 Break)
	5. Application of SAB on Cu/LCP Laminate H. Okayama, K. Nanbu, K. Saijo, Toyo-kohan Co. Ltd.; Tadatomo Suga, The University of Tokyo / Japan 6. Application of SAB on Wafer Bonding at Room Temperature H. Takagi, AIST / Japan 7. SAB Method for Bonding of Ionic Wafers at Room Temperature M. R Howlader, McMaster University, T. Suga, The University of Tokyo Canada / Japan 8. Application of SAB on MEMS Packaging H. Okada, T. Itoh, T. Suga, The University of Tokyo / Japan (17:20)	FB4: Advanced Substrate & Interposer 1. A New Fine Patterning Method for LTCC Electrode Used with Photo-Patterned Dry Film F. Uchikoba, K. Yamashita, Nihon University / Japan 2. Preparation and Properties of LTCC/Ag and LTCC/Cu Y. Liu, Tsinghua University, J. Tang, National Institute for Materials Science, Y. Wang, J. Ma, Tsinghua University / China, Japan 3. Development of LTCC(Low Temperature Co-fired Ceramics) Materials with High Mechanical Strength S. Kawai, Kyocera / Japan 4. LTCC Multi-layer Substrate Utilized with Ink-jet Printed Silver Layers and UV Laser Drilled Micro Vias T. Tanaka, KOA / Japan
17:45		