April 20 (Fri.)

9:30

FA1: Reliability and Testing

Chairperson: M.-H. Tseng (Industrial Technology Research Institute)
O. Yamada (Hitachi)

1. Development of the Probing Technology to a Very Fine Pitch and a Very Small Area
   M. Tanioka, M. Sunohara, T. Sato, K. Takahashi,
   Association of Super-Advanced Electronic Technologies (ASET) / Japan
2. 3-Dimension Measurement Sensor
   A. Tanuma, Anritsu / Japan
3. Advanced Moisture Diffusion and Vapour Pressure Modeling
   E.H. Wong, R. Rajoo, T.B. Lim, K.H. Lee*, S.W. Koh*,
   Institute of Microelectronics, *National University of Singapore / Singapore
4. Supply Current Test for Pin Opens in CMOS Logic Circuits
   M. Hashizume, A. Tsuji, M. Ichimiya, H. Yotsuyanagi, T. Tamesada,
   The University of Tokushima / Japan
5. Estimation of Fall Impact Strength for BGA Solder Joints
   T. Sogo, S. Hara, Toshiba / Japan
6. A Study on the Thermal Fatigue Characteristics of Microelectronic Packaging Solder Joints
   W. Qian, C. Guohai, H. Le, M. Jusheng, Tsinghua University / China

FB1: Substrates (3)

Chairperson: J.-K. Kim (Hong Kong University)
S. Oka (Mitsubishi Electric)

1. **Design and Manufacturing Factors of Micro-via Buildup Substrate Technologies (Invited)**
   Y. Tsukada, IBM Japan / Japan
2. Selection and Evaluation of Materials for Future System-on-package Substrate
   K. Shinotani, P. Raj, H. Agarwal, V. Sundaram, S. Bhattacharya, S. Zama,
   J. Lu, C. Zweben, G. White, R. Tummala,
   Georgia Institute of Technology / U.S.A.
3. Influences of Epoxy Dielectrics on Seeding Surface Used in Build-up Multilayers
   P. Jalonen, A. Tuominen, Tampere University of Technology / Finlamd
4. Ultra Fine Line Formation Processing for Advanced Build-up Package
   K. Kobayashi, Shinko Electric Industries / Japan
5. Study of Blind Via Hole of Build-up PWB
   E. Hirata, CMK / Japan
6. Cu Direct Laser Drilling Technology for Printed Circuit Boards
   K. Arai, Hitachi Via Mechanics / Japan

12:00 LUNCH TIME

13:00

FA2: Design and Simulation

Chairperson: E-H. Wong (Institute of Microelectronics)
S. Kitajo (NEC)

1. Area-distributed I/O Pad Design
   Y.-J. Huang, S.-L. Fu, I-Shou University / Taiwan
2. Two-dimensional Array Layout for Low Power NMOS 4-phase Dynamic Logic
   M. Furuie, Osaka University / Japan
3. Drop-simulation of Electronic Boards Mounted with CSPs
   I. Hirata, Y. Yoshida, I. Morisaki, NEC / Japan
4. A Greedy Router Based on Maze Router and Genetic Algorithm
   A. Kanasugi, Saitama University / Japan
5. A Placement Method Based on Boundary Method and Genetic Algorithm
   A. Kanasugi, Saitama University / Japan

FB2: Materials (2)

Chairperson: P. Miodushevsky (Powerco S.p.A.)
I. Kaneko (Musashi Institute of Technology)

1. The Vacuum Furnace for a Transparent Dielectric Layer
   M. Yokoe, Noritake Kizai /Japan
2. Preparation of Nobel Metals Fine Particles by Aerosol Process
   N. Iida, Noritake Kizai /Japan
3. Determination of Specific Contact Resistance between Electrode and Resistor Material for Fabrication of Low Value Resistor
   S. Ibaraki, S. Okada, M. Nakao, Y. Onuma, K. Kamimura, H. Ohe*,
   T. Sakuma*, Shinshu University, *KOA / Japan
4. The Performance and Dimension Control of Copper Alloy for Etching Applications
   H. Le, L. Chao, M. Jusheng, Tsinghua University / China
5. Preparation of Anodized Film on Metal Substrate
   Z. Jiman, M. Jusheng, Tsinghua University / China

15:05 COFFEE BREAK

15:25

FA3: Interconnection (2)

Chairperson: J. Simon (Technische Universtitat Berlin)
I. Watanabe (Hitachi Chemical)

1. Plasma Cleaning for Bonding
   R. Nickerson, AST Products / U.S.A.
2. Solder Fatigue Reliability of Chip Scale Package for Double Sided Surface Mount
   M. Amagai, Texas Instruments Japan / Japan
3. Effect of Solder Mixture on Joint Reliability of Repaired Components
   T. Nakashima, Sharp / Japan
4. Development of Flip-chip Mounting Process by Metallic Joint which Uses Ultrasonic Wave Energy
   K. Higashi, K. Ushirakawa, Matsushita Electric Industrial / Japan
5. Development of the Non-flux Solder Joint Technology
   R. Okada, Sumitomo Bakelite / Japan

FB3: High Speed/High Frequency Packaging

Chairperson: P. Barnwell (Heraeus)
T. Sudo (Toshiba)

1. Measurement Potential Swing by Electric Field on Package Transmission Lines
   K. Otsuka, T. Usami*, Y. Ohdate*, Y. Ikemoto**,
   Meisei University, *University of Tokyo, **Fujitsu / Japan
2. The Polymer Stud Grid Array (PSGA) Package : Test and Electrical Characterization for RF Applications
   A. Chandrasekhar, P. Pieters, K. Vaesen, E. Beyne, W. De Raedt,
   B. Nauwelaers, IMEC vzw / Belgium
3. Microwave Glob-top and Flip-chip with GaAs' MMICs for Space Applications
   C. Drevon, P. Monfraix, S. George, J. Cazaux,
   Alcatel Space Industries / France
4. Dual Band Antenna Switch Modules with Bare SAW Chips Mounted on LTCC
   F. Uchikoba, TDK / Japan
5. PCB Layout Dependence of Radiated Emissions
   H. Sasaki, T. Harada, T. Kuriyama, NEC / Japan

17:30