Advance Program

# ICEP-IAAC 2025

## 2025 International Conference on Electronics Packaging and iMAPS All Asia Conference

## April 15-19, 2025

## Wakasato Municipal Cultural Hall Nagano, Japan

**Sponsored by IEEE EPS, IEEE EPS Japan Chapter, iMAPS and SMTA**

**Welcome to ICEP-IAAC2025**

On behalf of the Organizing Committee, it is with great pleasure that we welcome you to the 24th International Conference on Electronics Packaging in conjunction with the iMAPS All Asia Conference (ICEP-IAAC2025). This esteemed event will take place at the Wakasato Municipal Cultural Hall in Nagano City from April 15 to 19, 2025.

The International Conference on Electronics Packaging (ICEP) is organized by the Japan Institute of Electronics Packaging (JIEP) and is technically co-sponsored by the IEEE Electronics Packaging Society (EPS), the IEEE EPS Society Japan Chapter, the Surface Mount Technology Association (SMTA), and the International Microelectronics Assembly & Packaging Society (IMAPS). Since its inception as the International Microelectronics Conference (IMC) in 1980, this event has undergone several transformations—from the IEEE International Electronic Manufacturing Technology Symposium (IEMT) to the annual IEMT/IMC starting in 1997—ultimately adopting the name ICEP in 2001.

We are exceptionally proud to host the IAAC event in Nagano, an esteemed occasion that takes place every three years in Japan. This year, the conference will begin with an IAAC session centered on the theme "3D Chiplet Technologies for Automotive/AI Applications." This session promises to provide groundbreaking insights into packaging, serving as the inaugural event of ICEP-IAAC2025.

ICEP-IAAC2025 is emerging as a premier conference in the field of electronics packaging, bringing together leading global figures from the electronics industry, academia, and research institutions. The event will feature more than 230 oral and poster presentations, marking a record high for ICEP. This conference offers an excellent platform for researchers and engineers from academic and industrial spheres worldwide to tackle new challenges and explore future research directions in electronics packaging. The conference encompasses a broad array of topics, including advanced packaging, design, modeling and reliability, emerging technologies, high-speed wireless components, thermal management, interconnections, materials and processes, optoelectronics, power electronics, and more. Furthermore, ICEP's long-standing partners—iNEMI, IMPACT, ISMP, and Pan-Pacific—will present unique regional technology trends in their dedicated sessions. International Symposium on Dry Process (DPS) and the Advanced Metallization Conference (ADMETA) of the Japan Society of Applied Physics (JSAP) will also host sessions at ICEP-IAAC2025.

In closing, we extend our deepest gratitude to our sponsors, committee members, session chairs, authors, presenters, local organizers in Nagano, and especially the secretariat members, whose dedication over the years has been instrumental in planning this conference. We sincerely hope you enjoy the engaging talks and fruitful discussions at ICEP-IAAC2025, amidst the beautiful natural surroundings of Nagano City.

Taiji Sakai
General Chair, ICEP-IAAC 2025

# Tuesday, April 15

## ■ IAAC Special Session

### 3D Chiplet Technologies for Automotive/AI Applications

| | Room A |
|---|---|
| 13:00 | **Greeting**<br>Beth Keser, Zero ASIC, IMAPS Past President / US |
| 13:10 | **TBD**<br>Hisashi Kanazashi, Ministry of Economy, Trade and Industry / Japan |
| 13:30 | **Latest Status of on-Substrate Material Development for CoWoS Packaging**<br>Shimpei Yamaguchi, tsmc Japan 3DIC R&D Center / Japan |
| 14:00 | **Advanced Packaging Technologies in Memory Applications for AI Era**<br>Ki Ill Moon, SK hynix /Korea |
| 14:30 | **Enabling Power Efficient AI with Advanced Packaging**<br>Hajime Saiki, AMD / US |

| | Room A |
|---|---|
| 15:00 | **Chiplets and Advanced Packaging for AI Applications: Costs and Risks**<br>Amy Lujan, SavanSys Solutions / US |
| 15:30 | Break |
| 15:45 | **Developments in Advanced SoC Research for Automotive**<br>Nobuaki Kawahara, ASRA / Japan |
| 16:15 | **Chiplets and Advanced Packaging for Automotive: Motivation and Opportunities**<br>Vikas Gupta, ASE / US |
| 16:45 | **Chiplets in Automotive Electronics : Opportunities and Challenges**<br>Andreas Grassmann,Infineon Technologies / Germany |

# Wednesday, April 16

ICEP-IAAC 2025 Advance Program

| | Room A | Room B | Room C | Room D | Room E |
|---|---|---|---|---|---|
| 9:30<br>11:10 | **WA1: iNEMI Session**<br>**WA1-1 <Session Invited>**<br>**A Study of Applying AI in Electronic Manufacturing**<br>Feng Xue[1], Masahiro Tsuriya[2], [1]IBM / Singapore, [2]iNEMI / Japan<br>**WA1-2**<br>**The Study of Glass Core Substrates Warpage**<br>Kang Eu Ong[1], Junko Konishi[2], Yoichiro Sato[2], Tatsuro Yoshida[3], Kei Murayama[3], Makoto Tsukahara[3], Haley Fu[4], [1]Intel Technology / Malaysia, [2]AGC, [3]Shinko Electric Industries / Japan, [4]iNEMI / China<br>**WA1-3**<br>**Thermomechcanical FEM Analysis of Sn-Bi Solder Joint During Temperature Cycling for Fine Pitch 1$^{st}$ Level Interconnect**<br>Toyohiro Aoki[1], Yasuharu Yamada[1], Sayuri Kohara[1], Gokhale Shripad[2], Sze Pei Lim[3], Russell Kastberg[4], Masahiro Tsuriya[5], [1]IBM Research – Tokyo / Japan, [2]Intel / US, [3]Indium / Malaysia, [4]IBM / US, [5]iNEMI / Japan<br>**WA1-4**<br>**Effect of Interfacial Wetting on First Level Interconnect Joint Formation for Low Temperature Solders-iNEMI Project**<br>Shripad Gokhale[1], Edvin Cetegen[1], Rui Zhang[1], Sze Pei Lim[2], Russell Kastberg[3], Toyohiro Aoki[4], Masahiro Tsuriya[5], [1]Intel / US, [2]Indium / Malaysia, [3]IBM Infrastructure / US, [4]IBM Research – Tokyo, [5]iNEMI / Japan | **WB1: Cu Interconnection**<br>**WB1-1**<br>**Influence of Geometrical Design Based on Copper Direct Bonding Process**<br>Koharu Yuzawa[1], Hideki Kitada[2], [1]Shima Shima Production, [2]K. R. C. Group / Japan<br>**WB1-2**<br>**Reducing Electrical Resistivity of Copper-CNT Composite Film for High-Ampacity Back End of Line and Interconnection**<br>Y. Takeishi, K. Yasuda, Osaka University / Japan<br>**WB1-3**<br>**Elemental Characterization for Electroless Cu Layer of Stacked Micro-via in Substrate by STEM and ToF-SIMS**<br>M. Nishijima[1], M. C. Hsieh[1], Z. Zhang[1], A. Suetake[1], R. Okumuara[1], H. Yoshida[1], C. Chen[1], H. Seto[2], Y. Kitahara[2], K. Hashizume[2], K. Yamanaka[1], K. Suganuma[1], [1]Osaka University, [2]Okuno Chemical Industries / Japan<br>**WB1-4**<br>**Thermo-mechanical Reliability of Ag and Cu Joint Stucture with EMC Molding**<br>YehRi Kim[1,2], Dongjin Kim[1], [1]KITECH, [2]Korea University / Korea | **WC1: Advanced Packaging-1**<br>**WC1-1 <Session Invited>**<br>**Wafer Bonding Advances & 3D Applications**<br>Hiroshi Yamamoto, EVG / Japan<br>**WC1-2**<br>**Advanced Packaging Activity at Arizona State University**<br>Hongbin Yu, Arizona State University / US<br>**WC1-3**<br>**Development of Fine-Pitch Cu-Cu Hybrid Bonding on Face-to-Back Structure for Three-Layer WoWoW: Impact of Wafer-Warpage on Wafer Bonding Properties**<br>Yukako Ikegami, Kengo Kotoo, Kan Shimizu, Yoshihisa Kagawa, Hayato Iwamoto, Sony Semiconductor Solutions / Japan<br>**WC1-4**<br>**Low-Temperature Cu/Cu Hydrophilic Bonding Using Ar Ion Beam Activation**<br>J. Wang[1,2,4], K. Takeuchi[3], M. Kubota[1,2], M. Kawano[1,2], T. Takagi[1,2], M. Niwa[1,2], T. Kuroda[1,2], T. Suga[1,2,4], [1]The University of Tokyo, [2]Research Association for Advanced Systems, [3]Tohoku University, [4]Meisei University / Japan | **WD1: Emerging Technologies**<br>**WD1-1**<br>**Packaging Design and Manufacturing of an Implantable Episclera Surface Stimulator**<br>Mian Tao, Chi-Chuen Jeffery Lo, Chi-Ying Tsui, Shi-Wei Ricky Lee, The Hong Kong University of Science and Technology / Hong Kong<br>**WD1-2**<br>**Cancelled**<br>**WD1-3**<br>**3D Miniaturization of Magnetic-Assisted Capsule Endoscope Using Mass-Transfer Cu Pillar Pin Assembly and Vacuum Printing Encapsulation**<br>Li-Cheng Shen[1], Sing Wu[2], Ming-Hung Chang[1], Chao-Hsuan Wang[1], Tai-Lin Wu[1], Hung-Yi Tsai[1], Chung-Ping Chang[1], Kuan-Ying Shen[1], Hawk Yeh[2], [1]Universal Global Scientific Industrial, [2]Insight Medical Solutions / Taiwan<br>**WD1-4**<br>**Proposal of a Multi-Layered Indoor Spatial Coordinate Definition Method and Compact Detection Module Using 5th Generation Mobile Communication System and Sensors**<br>Maho Terashima, Nobuaki Hashimoto, Suwa University of Science / Japan | **WE1: DMR-E-1**<br>**WE1-1**<br>**Power Integrity Improvement for CoWoS-L® Using Simulation-Based Modeling of Deep Trench Capacitor 1100 fF/mm$^2$**<br>Tzu-Yu Huang, Michael Yu, Jhen-Hong Lin, Mochtar Chandra, Christine Bair, L.C. Hung, James Chen, Taiwan Semiconductor Manufacturing / Taiwan<br>**WE1-2**<br>**Study of New Preconditioning for Solderability Testing**<br>Takaaki Sensui, Hideyuki Nagai, TDK / Japan<br>**WE1-3**<br>**A Machine Learning Model for Vickers Hardness of Sn-In-X Low-Temperature Solder**<br>Hao-Wei Kuo, Yu-chen Liu, National Chen Kung University / Taiwan<br>**WE1-4**<br>**Improved Electrical Reliability Within EMI-Shielding Case for the Assembly of Advanced Miniaturized Electronic Packages**<br>Masashi Nakahama[1], Akihiro Kiyosue[1], Mutsuharu Tsunoda[1], Morgana Ribas[2], [1]MacDermid Performance Solutions Japan / Japan, [2]MacDermid Alpha Electronics Solutions India / India |
| 11:10<br>11:20 | **Break** | | | | |
| 11:20<br>13:00 | **WA2: IMPACT Session**<br>**WA2-1 <Session Invited>**<br>**Alloying Effect on High Reliability Solder Materials**<br>Albert Tzu-Chia Wu[1], Wei-Ting Lin[1], Kelvin Li[2], Kuo-Shu Lin[2], Chang-Meng Wang[2], [1]National Central University, [2]Shenmao Technology / Taiwan<br>**WA2-2 <Session Invited>**<br>**Evaluation of Energy Dissipation Associated to Interface Debonding in Redistribution Interconnect**<br>Tz-Cheng Chiu, Shih-Chen Lin, National Cheng Kung University / Taiwan<br>**WA2-3 <Session Invited>**<br>**The trend of Heterogeneous Integration for GAI**<br>Dyi-Chung Hu, SiPlus / Taiwan<br>**WA2-4 <Session Invited>**<br>**Investigating the Electromigration Behavior Within Copper Redistribution Line Using Numerical Simulation Methods**<br>Tai-Yu, Pan[1], Min-Yan, Tsai[2], Wen-Dung, Hsu[1], [1]National Cheng Kung University, [2]ASE Group / Taiwan | **WB2: Cu-Cu Bonding**<br>**WB2-1**<br>**Investigation of Bonding between Nanotwinned Cu and Nanocrystalline Cu**<br>Po-Hung Lai, Chih Chen, National Yang Ming Chiao Tung University / Taiwan<br>**WB2-2**<br>**Optimizing Cu-Cu Bonding Strength in Nanotwinned Cu Films Through Plasma-Induced Surface Roughening**<br>Ming-Chieh Chen, Chih Chen, National Yang Ming Chiao Tung University / Taiwan<br>**WB2-3**<br>**Light Exposure Pre-treatment for Copper-to-Copper Direct Bonding**<br>Yu-Cheng Ke, Yao-Wen Zhang, Jenn-Ming Song, National Chung Hsing University / Taiwan<br>**WB2-4**<br>**Nanocrystalline Cu-Cu Bonding Arrays for High-Density Integrated Circuits**<br>Zi-Ting Ye, Shichen Xie, King-Ning Tu, Yingxia Liu, City University of Hong Kong / Hong Kong | **WC2: Advanced Packaging-2**<br>**WC2-1**<br>**Regulating Sn Grain Orientations in Solder Joints Through CoSn$_3$**<br>Xinjie Wang, Hiroaki Tatsumi, Hiroshi Nishikawa, Osaka University / Japan<br>**WC2-2**<br>**Glass to Glass Joint by Low Temperature Soldering Using Localized Induction Heating Process**<br>Chi Hsuan Lin[1], Hiroaki Tatsumi[1], Jenn Ming Song[2], Hiroshi Nishikawa[1], [1]Osaka University / Japan, [2]National Chung Hsing University / Taiwan<br>**WC2-3**<br>**Effect of Bi on Properties of Sn-9Zn Alloy for Interconnections**<br>Hao-Zhe Kao, Chih-Ming Liang, Yu-An Shen, Feng Chia University / Taiwan<br>**WC2-4**<br>**Design High Shear Strength Sn-Bi-X Low-Temperature Solders on Cu Substrate Using a Machine Learning Approach**<br>Pei-Zhen Wu, Yu-chen Liu, National Cheng Kung University / Taiwan | **WD2: Polymer Materials**<br>**WD2-1 <Session Invited>**<br>**A Liquid Epoxy Encapsulant With Excellent Weather Resistance, Long-Term Reliability and Casting Properties**<br>Satoshi Osawa, Takayuki Kajihara, Toshio Suetsugu, Tatsuya Ikeda, NIHON GOSEI KAKO / Japan<br>**WD2-2**<br>**Effect of Silica Fillers on the Curing Reaction of Epoxy–Imidazole Thermoset Resin**<br>K. Naka[1], Y. Furushima[1], T. Hirano[1], Y. Taguchi[1], H. Torigoe[2], T. Takao[2], A. Takase[2], T. Nousou[2], Y Ishikawa[2], K. Ishii[2], [1]Toray Research Center, [2]Sanyu Rec / Japan<br>**WD2-3**<br>**Electrical Conductivity Variations of Stretchable Printed Wires Examined from Hierarchic Deformation Behavior**<br>Masahiro Inoue, Rintaro Yamamoto, Gunma University / Japan<br>**WD2-4**<br>**Acceleration of Silver Micro-Flake Sintering to Enhance Interconnection Integrity Using a Flexible Epoxy-Based Binder**<br>Takanori Fukushima, Masahiro Inoue, Gunma University / Japan | **WE2: DMR-E-2**<br>**WE2-1**<br>**Rifined Measurement of the Specific Contact Resistivity and Reliability at the Interface between Bismuth Telluride and Metals**<br>A. Katsura[1], M. Tsurumoto[1], Y. Hirose[1], D. Micucci[2], T. Sugahara[1], [1]Kyoto Institute of Technology / Japan, [2]Politecnico di Torino / Italy<br>**WE2-2**<br>**HV-H3TRB Evaluation of Ag and Cu Sintering Paste for Double Sided Sintered Power Devices**<br>Felix Steiner[1], Dai Ishikawa[2], Hideo Nakako[2], Thomas Blank[1], [1]Karlsruhe Institute of Technology / Germany, [2]Resonac / Japan<br>**WE2-3**<br>**A Mesh Size Searching Method in WLP Reliability Prediction with Fixed Coffin-Manson Parameters**<br>Y. T. Su, K. N. Chiang, National Tsing Hua University / Taiwan<br>**WE2-4**<br>**Prototype of Heating Device for Low-Temperature Cooking Using Dielectric Heating**<br>K. Imai, Y. Furuyama, K. Kuramochi, T. Yamamoto, Tokyo University of Science / Japan |
| 13:00<br>13:50 | **Lunch** | | | | |
| 13:50<br>14:30 | **Award Ceremony** | | | | |
| 14:30<br>14:40 | **Break** | | | | |
| 14:40<br>15:40 | **Keynote Lecture I:** Brightening the Future with Advanced Semiconductor Packaging Technologies<br>Yasushi Araki, SHINKO ELECTRIC INDUSTRIES | | | | |
| 15:40<br>16:40 | **Break / Poster Session** | | | | |
| 16:40<br>17:40 | **Keynote Lecture II:** Digital Twins in Data Center Cooling: Meeting AI Demands With Smart Design and Innovation<br>Ali Heydari, NVIDIA | | | | |
| 17:40<br>17:45 | **Introduction to 2026** | | | | |
| 18:30<br>20:30 | **Welcome Reception** | | | | |

| | Room A | Room B | Room C | Room D | Room E |
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| 8:30<br>9:30 | **Keynote Lecture III:** Beyond Moore's Law: Semiconductor Packaging in the Chiplet Revolution<br>Yasumitsu Orii, Rapidus | | | | |
| 9:30<br>9:40 | **Break** | | | | |
| 9:40<br><br>11:20 | **TA1: ADMETA/DPS Session**<br>**TA1-1 <Session Invited>**<br>**Deposition of Dielectric Films From Plasma-Generated Aerosols**<br>Zachary Holman, Arizona State University / US<br>**TA1-2 <Session Invited>**<br>**Advanced Plasma Etching Technology for Cutting-Edge Devices**<br>Michikazu Morimoto, Hitachi High-Tech / Japan<br>**TA1-3 <Session Invited>**<br>**Multilayer Graphene Synthesis by Microwave Plasma CVD for Interconnect Application**<br>Takashi Matsumoto, Tokyo Electron Technology Solutions / Japan<br>**TA1-4 <Session Invited>**<br>**Cultural Fusion ?**<br>Tadashi Fukuda, Tech Extension / Japan | **TB1: Advanced Metallic Materials**<br>**TB1-1**<br>**Development of Industrial Purification Methods for Silver Nanowires Used as Transparent Conductive Materials**<br>K. Sato[1,2], S. Kumon[1], J. Balachandran[2], Y. Sutou[2], [1]DOWA HOLDINGS, [2]Tohoku University / Japan<br>**TB1-2**<br>**Phase Equilibrium of the Fe-Sn-Zn Ternary System at 270°C**<br>Ssu-Chi Huang, Hsing-Tieh Lee, Yu-Pin Hsieh, Yee-Wen Yen, National Taiwan University of Science and Technology / Taiwan<br>**TB1-3**<br>**Copper Nano/Fine Particles as Joining Materials for Low Temperature Sintering**<br>Tetsu Yonezawa, Hokkaido University / Japan<br>**TB1-4**<br>**Cost-Effective and Low-Temperature Sintering of Oxidized Copper Nanoparticles for Power Electronics**<br>Tetsu Yonezawa, Hokkaido University / Japan | **TC1: SMTA/Pan Pacific Session**<br>**TC1-1 <Session Invited>**<br>**A Novel Expansion Process for FO-WLP Using Tape Expansion, Self-Assembly, and Tape Frozen Detachment Technique**<br>Shinya Takyu, LINTEC / Japan<br>**TC1-2 <Session Invited>**<br>**Conductive Cu Paste as a Via Filling Material for Through Glass Via (TGV)**<br>Yoshinori Ejiri, Masumi Sakamoto, Chiaki Shimizu, Naoyuki Kikuchi, Futoshi Oikawa, Masayoshi Nishimoto, Seiji Kai, Hiroshi Uragami, Resonac / Japan<br>**TC1-3 <Session Invited>**<br>**Chip-to-Wafer Polymer Hybrid Bonding for low-temperature process**<br>Takenori Fujiwara, Toray Industries / Japan | **TD1: Solder Interconnect**<br>**TD1-1**<br>**High-Speed Solder Ball Shear Test and Component Shear Test for Evaluating the Robustness of Solder Joints Under Different Reflow Peak Temperature**<br>Y. Y. Chen, Y. S. Zou, Vance Liu, M. H. Chung, C. L. Gan, Micron Technology / Taiwan<br>**TD1-2**<br>**Multi Scale Micromechanical Testing for New Polymer Core Solder Ball (PCSB) Interconnections Reliability in Operating Conditions**<br>Irati Malkorra[1], Sergio Sao-Joao[1], Guillaume Kermouche[1], Sébastien Bucher[2], [1]Mines Saint-Etienne, [2]IREIS / France<br>**TD1-3**<br>**Enhanced Self-Propagating Exothermic Reaction Bonding With Nanostructured Cu/Sn Interlayer**<br>Han Jiang[1,2], Changqing Liu[2], Jingyu Chen[3], Yaohua Xu[1], [1]Anhui University / China, [2]Loughborough University, [3]The University of Sheffield / UK<br>**TD1-4**<br>**Enhanced Electrochemical Migration Resistance of Fine-Pitch Nano-Sized Ag Interconnects by Self-Assembly Monolayers**<br>Fan-Yi Ouyang, Chia-Hung Tsou, Wan-Hsuan Lin, Chien-Cheng Chiang, National Tsing Hua University / Taiwan | **TE1: Optoelectronics-1**<br>**TE1-1 <Session Invited>**<br>**All-Photonics-Function Embedded Package Substrate Using 2.3D RDL Interposer for Co-Packaged Optics**<br>Akihiro Noriki[1], Hirotaka Uemura[2], Haruhiko Kuwatsuka[1], Naoki Matsui[2], Reona Motoji[2], Dan Maeda[2], Tomoya Sugita[2], Fumi Nakamura[1], Satoshi Suda[1], Takayuki Kurosu[1], Takeru Amano, [1]AIST, [2]Kyocera / Japan<br>**TE1-2**<br>**A Simulation Study for Optimal Conditions of Single-Mode Polymer Optical Waveguides in Chip-To-Chip Connections**<br>Hiroki Ito, Yuji Furuta, Kenji Yanagisawa, Masaharu Kato, Hisashi Kaneda, Tomoharu Fujii, Shinko Electric industries / Japan<br>**TE1-3**<br>**Refractive Index Profile Analysis of Single Mode Polymer Optical Waveguide by Using Propagation-Mode Near Field Method**<br>Masaki Matsumoto, Tomoharu Fujii, Kazuhiro Yoshida, Shinko Electric industries / Japan |
| 11:20<br>11:30 | **Break** | | | | |
| 11:30<br><br>13:10 | **TA2: Glass PKG-1**<br>**TA2-1 <Session Invited>**<br>**Glass Packaging Markets and Critical Issues to Solve**<br>E Jan Vardaman, TechSearch International / US<br>**TA2-2**<br>**Advanced Fabrication Techniques for Through Glass via (TGV) in Glass Core Substrates for Hetrogeneous Integration of 2.5D/3D Advanced Packaging Applications**<br>Venugopal Govindarajulu[1], Coby Tao[1], Vengal Jalagam[1], Keshav Chandran[1], Katsumi Yoneda[2], Zia Karim[1], [1]Yield Engineering Systems / USA, [2]Yield Engineering Systems / Japan<br>**TA2-3**<br>**Driving Efficiency in Advanced Packaging: TGV Tool Concepts and Supply Chain Impacts**<br>Richard Noack, Nils Anspach, Daniel Dunker, Roman Anspach, Rafael Santos, LPKF Laser & Electronics / Germany<br>**TA2-4**<br>**Pre-treatment for Adhesion Layer in Panel-Level Sputtering Applying an Improved Linear Ion Source**<br>A. Higashi, A. Ihori, T. Yuze, T. Terasawa, Y. Morikawa, ULVAC / Japan | **TB2: Low Temperature Solder Materials**<br>**TB2-1**<br>**Nanoindentation Study of Phases in Near-Eutectic Sn-Bi Alloy**<br>Xin Fu Tan[1], Viola Paul[2], Takahito Ohmura[2], Stuart D. McDonald[1], Kazuhiro Nogita[1], [1]The University of Queensland / Australia, [2]NIMS / Japan<br>**TB2-2**<br>**Tensile Properties of Sn-37wt%Bi and Sn-57wt%Bi at Low Temperatures**<br>Xiaozhou Ye, Stuart D McDonald, Xin Fu Tan, Kazuhiro Nogita, The University of Queensland / Australia<br>**TB2-3**<br>**Planar Geometry Solder Study of Alloying Effects on Sn-Bi Electromigration**<br>Prabjit Singh[1], L. Palmer[1], T. Wassick[1], R. F. Aspandiar[2], B. Franco[2], L.A. Swaminathan[2], H. Fu[3], V. Vasudevan[4], A. Allen[5], K. Howell[6], K. Murayama[7], H. Zhang[8], A. Lifton[9], T. Munson[10], S. Middleton[10], M. Sarangapani[11], [1]IBM, [2]Intel / US, [3]iNEMI / China, [4]Dell Technologies, [5]HP / US, [6]Nihon Superior, [7]Shinko Electric Industries / Japan, [8]Indium, [9]MacDermid Alpha Electronics Solutions, [10]Foresite / US, [11]Heraeus Materials Singapore / Singapore<br>**TB2-4**<br>**Mechanical Tensile Behaviors of Sn-Bi Lead-Free Solder Alloys under Different Strain Rates and Temperatures**<br>Min-Cheng Yu, Nien-Chun Lin, Hsin-Chih Shih, Ching-I Tsai, Chin-Li Kao, Chen-Chao Wang, C.P. Hung, Wen-Fung Pan, ASE / Taiwan | **TC2: ISMP Session**<br>**TC2-1 <Session Invited>**<br>**2.xD Advanced Packaging with Bridge Die Platforms: Development, Structure, and Reliability**<br>Jayden Donghyun Kim, Jae-Sung Lim, Sanggyu Jang, Jin-Wook Jang, Yong-Nam Koh, HANA Micron / Korea<br>**TC2-2 <Session Invited>**<br>**The Study on Ultra-Precision Surface Measurement Technologies in The Hybrid Bonding Process**<br>Joonho You, nexensor / Korea<br>**TC2-3 <Session Invited>**<br>**Nanomechanical Modeling of Fracture and Plasticity in Metallic Multilayers During Thermal Cycles**<br>Ill You, Seoul National University / Korea<br>**TC2-4 <Session Invited>**<br>**Single-Additive Cu Electrodeposition for Defect-Free TSV Filling**<br>Myung Jun Kim, Sungkyunkwan University / Korea | **TD2: Power Electronics-1**<br>**TD2-1**<br>**Issues of Using Unsaturated Heating Time for Transient Thermal Measurement Part 3**<br>Shuhei Fukunaga[1], Tomoaki Hara[2], Tsuyoshi Funaki[1], [1]Osaka University, [2]Siemens / Japan<br>**TD2-2**<br>**Large-Area Bonding for Direct Cooling for Allpications in Power Inverters**<br>Shin-Il Kim[1], Yong-Ho Ko[1,2], Dongjin Kim[1], [1]KITECH, [2]University of Science Technology / Korea<br>**TD2-3**<br>**Numerical and Experimental Investigations on Thermo-Stable Reliability of a Physical Property-Controlled Type High-Heat Dissipation Spacer for Double-Side Cooling Power Modules**<br>Dongjin Kim[1], Byeong Chan Kim[1], Yeh Ri Kim[1], Kue Jin Han[2], Taeseong Han[2], [1]KITECH, [2]KOSTECSYS / Korea<br>**TD2-4**<br>**Thermal Stability of Vertical Type Shunt Resistors for Use in Double Side Cooling SiC Power Modules**<br>Dongjin Kim[1], Yeh Ri Kim[1], Byeong Chan Kim[1], Kue Jin Han[2], Taeseong Han[2], [1]KITECH, [2]KOSTECSYS / Korea | **TE2: Optoelectronics-2**<br>**TE2-1**<br>**Reflowable Ceramic Multifiber Ferrule for Co-Packaged Optics**<br>Alexander William Setiawan Putra, Kentaro Matsuda, Motohito Takezaki, Hakusan / Japan<br>**TE2-2**<br>**Novel Passive Alignment Implementation using 41° Cleaved Fiber Array for Silicon Photonic Micro-Transceiver**<br>Michiyo Kubo, Shigeru Kobayashi, Koichi Takemura, Makoto Kuwata, Kazuhiko Kurata, AIO Core / Japan<br>**TE2-3 <Session Invited>**<br>**Fabrication and Transient Optical Response of 910nm Broadband Near-IR Remote Phosphor-Converted LED**<br>Atsushi Okuno[1], Jang Uk An[2], [1]Green Planets / Japan, [2]ALLIX / Korea |
| 13:10<br>14:00 | **Lunch Time** | | | | |

## Contact Information

Please contact for any inquiries about:


**Registration**

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**Conference Programs**

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| | Room A | Room B | Room C | Room D | Room E |
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| 14:00<br><br>15:40 | **TA3: Glass PKG-2**<br>**TA3-1 <Session Invited>**<br>**High AR TGV Direct Wet Cu Metallization on Glass**<br>A. Okitmoto[1], T. Onishi[1,2], K. Inoue[1], M. Takayama[1], [1]Koto Electric / Japan, [2]Grand Joint Technology / Hong Kong<br>**TA3-2**<br>**Development of Acid Copper Electroplating Chemicals for Advanced Packaging with TSV and TGV**<br>Nobuaki Nagano, Shota Suzuki, Ryo Aizawa, Yusuke Suga, Tetsuro Eda, JCU / Japan<br>**TA3-3 <Session Invited>**<br>**Acid Copper Plating Process for RDL Suitable for Glass Substrate**<br>Atsuya Yamaguchi, Kohei Imahase, Reito Kobayashi, Tetsuro Eda, JCU / Japan<br>**TA3-4 <Session Invited>**<br>**Integrated Low Temperature Based Glass Core Substrate Manufacturing Solutions Minimizing SeWaRe Type Failures**<br>Christian Buchner, SCHMID Group / Germany | **TB3: Materials for Hybrid Bonding**<br>**TB3-1**<br>**Enhancement of Bonding Strength Between Cured Polymer Dielectrics and $SiO_2$ by Plasma Activation Treatment**<br>Natsumi Sumito, Wataru Okada, Ryo Hayakawa, Satoshi Otsuka, Yuzo Nakamura, Yutaka Hisamune, Satoshi Inada, Mitsui Chemicals / Japan<br>**TB3-2**<br>**Hybrid Bonding of Cu and Manganin by Using VUV Irradiation**<br>Fu-Ling Chang[1,2], C. Robert Kao[1], Akitsu Shigetou[2], [1]National Taiwan University / Taiwan, [2]NIMS / Japan<br>**TB3-3**<br>**Surface Modification of Cu Native Oxide: Ag Displacement for Homogeneous Layering**<br>Shubhayan Mukherjee[1], Akitsu Shigetou[2], Shih-kang Lin[1], [1]National Cheng Kung University / Taiwan, [2]NIMS / Japan<br>**TB3-4**<br>**Dimensional Effects on Grain Size and Surface Orientation of Nanocrystalline Cu in $SiO_2$ Micro-Vias**<br>Te-Hao Chao, Huai-En Lin, Chih Chen, National Yang Ming Chiao Tung University / Taiwan | **TC3: Advanced Packaging-3**<br>**TC3-1**<br>**The Effect of Key Factors on 3D X-ray Imaging for Fan-Out Package**<br>Fan-Ju Hsiao, Yi-Sheng Lin, Cheng-Hsin Liu, ASE / Taiwan<br>**TC3-2**<br>**Chemical Identification of Foreign Matters in a Cavity Using Submicron Infrared Spectroscopy**<br>Michael K.F. Lo[1], Naoki Baden[2], Hanae Kobayashi[2], Norio Urayama[2], [1]Photothermal Spectroscopy / US, [2]Nihon Thermal Consulting / Japan<br>**TC3-3**<br>**In-Situ EBSD Tensile Behaviors of Pressured Silver Sintered Structures**<br>Ha-Young Yu, Min-Su Kim, Dongjin Kim, KITECH / Korea<br>**TC3-4**<br>**Simulation and Experimental Analysis of Capillary Underfill in 2.5d Multi-Chip Modules**<br>Chien-Ting Wu[1], Kazuki Noguchi[2], Yu-En Liang[1], Wei-Yu Lin[1], Zi-Hsuan Wei[1], Ching-Kai Chou[1], Leo Shen[1], [1]CoreTech System (Moldex3D) / Taiwan, [2]Sanyu Rec / Japan | **TD3: Power Electronics-2**<br>**TD3-1**<br>**Evaluating the Effect of Ion Implantation on Suppression of Stacking Fault Expansion in 4H-SiC by Raman Spectroscopy**<br>A. Myalitsin[1,2], V. Maeckel[2], T. Yoda[1], T. Ohba[1], [1]Institute of Science Tokyo, [2]ANVOS Analytics / Japan<br>**TD3-2**<br>**Non-destructive X-Ray Orientation Mapping of Die-Attach Solder Before and After Thermal Cycling Test**<br>Y. Hayashi[1], J. Kim[1], M. Yabashi[1], H. Tatsumi[2], [1]RIKEN SPring-8 Center, [2]Osaka University / Japan<br>**TD3-3**<br>**Power Cycle Testing, Behaviour of Clip-Sintered Bare Dies**<br>Felix Steiner[1], Janis Blank[1], Dai Ishikawa[2], Hideo Nakako[2], Thomas Blank[1], [1]Karlsruhe Institute of Technology / Germany, [2]Resonac / Japan<br>**TD3-4**<br>**Lower Inductance of POL Double-Layer Facing Structure Power Module**<br>Takumi Yumoto[1], Takumi Ikeda[1], Yoichi Nishihara[1], Keita Suzuki[2], Yoshikazu Takahashi[2], Koji Bando[1], [1]Shinko Electric Industries, [2]Tohoku University / Japan | **TE3: DMR-M-1**<br>**TE3-1**<br>**A Novel FOWLP Process Emulator for Predicting Multi-Step Accumulated Thermal-Mechanical Asymmetric Warpage Incorpreating Time-Dependent Plastic Effects**<br>Shang-Feng Hsu, Kuo-Shen Chen, National Cheng-Kung University / Taiwan<br>**TE3-2**<br>**Warpage Control Strategy of Embedded Die Packaging on SESUB Technology**<br>Wei-Hong Lai, Chun-Yu Yen, Chung-Hung Lai, Tsung-Yuan Yang, Chin-Li Kao, Chen-Chao Wang , ASE / Taiwan<br>**TE3-3**<br>**Micro-Bump Connection and Chip Warpage Control Using the Reflow Process**<br>T. Igarashi, M. Togawa, M. Nakazawa, H. Iwamoto, Sony Semiconductor Solutions / Japan<br>**TE3-4**<br>**Warpage Behavior of Three-Phase SiC MOSFET Power Module During Fabrication**<br>Y. H. Liao[1], H. C. Cheng[1], Y. L. Liu[1], K. S. Kao[2], T. C. Chang[2], [1]Feng Chia University, [2]ITRI / Taiwan |
| 15:40<br>16:00 | **Break** | | | | |
| 16:00<br><br>17:40 | **TA4: Heterogeneous Integration Roadmap**<br>**TA4-1 <Session Invited>**<br>**IIoT enabled by Heterogeneous Integration and AI**<br>Wei-Chung Lo, ITRI / Taiwan<br>**TA4-2 <Session Invited>**<br>**Scalable 3D Chiplet Integration for AI Inference Applications**<br>Farhang Yazdani, BroadPak / US<br>**TA4-3 <Session Invited>**<br>**Revolutionizing the Future: The Growth of Heterogeneous Integration, Chiplets, and Advanced Packaging**<br>Rozalia Beica, Rapidus Design Solutions / US<br>**TA4-4 <Session Invited>**<br>**TBD** | **TB4: Intermetallic Compound for Electronic Packaging**<br>**TB4-1**<br>**Phase Transitions of the η'-$Cu_6Sn_5$ Phase Under Electric Currents**<br>Shubhayan Mukherjee, Yu-chen Liu, Shih-kang Lin, National Cheng Kung University / Taiwan<br>**TB4-2**<br>**Intermetallic Compound Formation and Growth Behavior Between Ruthenium and Tin System**<br>Hsiu-mei Yang[1], Tzu-hsuan Huang[1], Yu-hsuan Lin[1], Min-cian Chen[2], Shih-kang Lin[1], [1]National Cheng Kung University, [2]Taiwan Semiconductor Manufacturing / Taiwan<br>**TB4-3**<br>**A Study on the Growth Kinetics and Hardness of IMCs in Au-In Joints**<br>Chih-Chia Bill Chang, C. R. Kao, National Taiwan University / Taiwan<br>**TB4-4**<br>**In-Situ Observations of Crack Propagation and Microstructure Evolution in a SAC305/Cu Solder Joint Using High-Voltage Electron Microscopy**<br>Kazuhiro Nogita[1], Xin F. Tan[1], Jiye Zhou[1], Stuart D. McDonald[1], Keith Sweatman[1,2], Flora Somidin[1,3], Hiroshi Maeno[4], Kazuhiro Yasuda[4], [1]The University of Queensland / Australia, [2]Nihon Superior / Japan, [3]University of Malaysia Perils / Malaysia, [4]Kyushu University / Japan | **TC4: Advanced Packaging-4**<br>**TC4-1**<br>**Micro Ball Mount Total Process in Wafer-Level and Panel-Level in Chip Preparation for Next on Large Panel-Level Package**<br>Jia Sang Weng, Cong-Wei Chen, Shih Yu Wang, Ping-Feng Yang, Jen-Kuang Fang, ASE / Taiwan<br>**TC4-2**<br>**Studies of the Twin Coherency on Electroless (111) Nanotwins**<br>Po-Shao Shih[1], I-En Chen[1], Chin-Li Kao[2], Yung-Sheng Lin[2], Yun-Ching Hung[2], C. R. Kao[1], [1]National Taiwan University, [2]ASE Group / Taiwan<br>**TC4-3**<br>**Smoothing of Plated Au Bumps Based on Template-Stripping for Low-Temperature Bonding**<br>Shogo Koseki[1], Kai Takeuchi[1], Le Hac Huong Thu[2], Takashi Matsumae[2], Hideki Takagi[2], Yuichi Kurashima[2], Takahiro Tsuda[3], Tomoaki Tokuhisa[3], Toshikazu Shimizu[3], Eiji Higurashi[1], [1]Tohoku University, [2]AIST, 3Kanto Chemical / Japan<br>**TC4-4**<br>**Superior Electrical Characteristics of Au-Sn Intermetallic Compound with Ultra-Thin Buffer Layer Structure in Eutectic Bonding Technology for 3D Integrated Circuits Applications**<br>Cheng-Yu Wei[1], Chiao-Yen Wang[1], Pei-Ru Lee[1], Mu-Ping Hsu[1], Yi-Chieh Tsai[2], Wun-Kai Wang[2], Kuan-Neng Chen[1], [1]National Yang Ming Chiao Tung University, [2]TXC / Taiwan | **TD4: Power Electronics-3**<br>**TD4-1 <Session Invited>**<br>**Wire Bondless WBG Power Devices With Sinterconnect Technology**<br>Ali Roshanghias, Silicon Austria Labs / Austria<br>**TD4-2**<br>**Cost-Performance Silver-Aluminum Composite Sinter Paste with Improved Joint Reliability in SiC Power Device Applications**<br>Chuantong Chen[1,2], Fupeng Huo[1], Hiroaki Miyake[2], Katsuaki Suganuma[1], [1]Osaka University, [2]Tokyo City University / Japan<br>**TD4-3**<br>**Cancelled**<br>**TD4-4**<br>**Investigates of Silver Sintered Process by Silver Thin Films and Nanotwinned Silver Thin Films**<br>Shin-Yi Huang[1], Yan-Cheng Lin[1], Ping-Chun Kao[2], Yung-Min Hsieh[1], Yu-Hua Wu[1], Fan-Yi Ouyang[2], Tao-Chih Chang[1], [1]ITRI, [2]National Tsing Hua University / Taiwan | **TE4: DMR-M-2**<br>**TE4-1**<br>**Silica Fillers Embedded in Epoxy Mold Compound Cause Inner Stress Concentration**<br>Ayumi Haginiwa[1], Masaya Ukita[1], Keisuke Wakamoto[1], Yuya Shitashige[2], Keizo Arai[2], Ken Nakahara[1], [1]ROHM, [2]Resinous Kasei / Japan<br>**TE4-2**<br>**Direct Observation of Copper Oxidation as a Cause of Delamination at the Interface of Copper and Epoxy Molding Compounds**<br>Keisuke Wakamoto, Masaya Ukita, Ayumi Haginiwa, Ken Nakahara, ROHM / Japan<br>**TE4-3**<br>**Thermomigration for Multi-Principal Element Solder with Low Melting Point**<br>Yifan Yao, Xingchao Mao, Yuanxing Duan, K. N. Tu, Yingxia Liu, City University of Hong Kong / Hong Kong<br>**TE4-4**<br>**Predictive Validity for Sintered Die-Attach Performance Based on Cross-Sectional Morphology**<br>Runhua Gao[1], Hiroaki Tatsumi[1], Takanori Kobatake[2], Minoru Ueshima[2], Hiroshi Nishikawa[1], [1]Osaka University, [2]Daicel / Japan |
| 17:40<br>19:10 | **Poster Session & Sponsors Exhibition** | | | | |

# ■Registration

### Registration Information

Early-Bird Registration Due: March 27th, 2025
Pre-Registration Due: April 15th, 2025
On-site registration is available from April 15th, 2025.

### Registration Fees

Fees are shown as “Early-Bird [On-Site]”. All registrations include complimentary conference proceedings and attendance to live sessions and receptions.

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| Members of JIEP/IEEE/iMAPS: | ¥45,000 [¥52,000] |
| Members of Partner Organizations: | ¥50,000 [¥57,000] |
| Non-Members: | ¥60,000 [¥67,000] |
| Students: | ¥20,000 [¥23,000] |
| Additional Welcome Reception Ticket: | ¥10,000 / person |

**Partner Organizations:** (to be confirmed)
Japan Electronics and Information Technology Industries Association / Japan Electronics Packaging and Circuits Association / Japan Jisso Technology Transfer Association
Japan Society of Powder and Powder Metallurgy / Japan Welding Society / Optoelectronics Industry and Technology Development Association
Smart Processing Society for Materials, Environment & Energy / The Electrochemical Society of Japan
The Institute of Electrical Engineers of Japan / The Institute of Electronics, Information and Communication Engineers / The Japan Society for Precision Engineering
The Japan Society of Applied Physics / The Society of Chemical Engineers, Japan / The Surface Finishing Society of Japan

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| 8:30<br>9:15 | **Keynote IV:** Recent Development Trend of FC-BGA Substrate With Chip-Let Structures Driven by HPC Applications<br>Genjin Mago, Ajinomoto Fine-Techno | | | | |
| 9:15<br>10:00 | **Keynote V:** Strategic Directions for Advanced Packaging<br>Subramanian S. Iyer, University of California, Los Angeles | | | | |
| 10:00<br>10:10 | **Break** | | | | |
| 10:10<br>11:50 | **FA1: Advanced Packaging and Thermal Management**<br>FA1-1<Session Invited> (50 min.)<br>**Innovations in Hybrid Bonding and Thermal Management for Advanced Packaging**<br>Kuan-Neng Chen, National Yang Ming Chiao Tung University / Taiwan<br>FA1-2<Session Invited> (50 min.)<br>**AI-Accelerated Multiscale Thermal & Mechanical Simulations for Advanced Packaging and IC Design**<br>Alexander J. Gabourie, DeepSim / US | **FB1: Process Glass/Plating**<br>FB1-1 <Session Invited><br>**JPCA Technology Roadmap for Glass Substrate**<br>Henry H. Utsunomiya, Interconnection Technologies / Japan<br>FB1-2 <Session Invited><br>**Low CTE Copper Electrodeposit**<br>Kazuo Kondo, Fine Feature Electrodeposition Research Laboratory / Japan<br>FB1-3<br>**Laser Applications in Micro-Machining of Glass Material Substrates**<br>Hsiang-Chen Hsu[1], Shih-Jeh Wu[1], Wen-Fei Lin[2], Shui-Cheng[1], [1]I-Shou University, [2]E&R Engineering / Taiwan<br>FB1-4<br>**Predicted Cu Plating Thickness Distribution in Fan-out Panel Level Package with Global/ Local Model**<br>Yi-Lun Hung, Yung-Sheng Lin, Min-Yan Tsai, Mingtzung Kuo, Ling-yuan Chang, Chen-Chao Wang, Ping-Feng Yang, Chin-Pin Hung, ASE Group / Taiwan | **FC1: Advanced Packaging-5**<br>FC1-1<br>**Elimination of Leakage in NaOH-activated $Cu/SiO_2$ Hybrid Bonding for Plasma-Free Surface Activation Scheme**<br>Huai-En Lin[1], Yu-Xiang Huang[1], Wei-Lan Chiu[2], Hsiang-Hung Chang[2], Chih Chen[1], [1]National Yang Ming Chiao Tung University / Taiwan, [2]ITRI / Taiwan<br>FC1-2<br>**Sub-100-nm Grain Size Electroplated Copper for Low-Temperature Bonding Applications**<br>Jian-Yuan Huang[1], Dinh-Phuc Tran[1], Kang-Ping Lee[1], Emile Kuo[2], Tsung-Chuan Chen[2], Yao-Tsung Chen[2], Stream Chung[2], Chih Chen[1], [1]National Yang Ming Chiao Tung University, [2]Chemleaders / Taiwan<br>FC1-3<br>**Sintered Cu-to-Cu Joints Using Cu Dendritic Structure Formed by a Dynamic Hydrogen Bubble Template with Cetyltrimethylammonium Bromide**<br>Ji-Hyun Kim, Hiroaki Tatsumi, Hiroshi Nishikawa, Osaka University / Japan<br>FC1-4<br>**Investigation of Cu-to-Cu Bonding Featuring Indium Passivation and a Tin Diffusion Barrier Layer**<br>Y. C. Tseng[1], Y. S. Lin[2], Y. C. Hung[2], C. R. Kao[1], [1]National Taiwan University, [2]ASE Group / Taiwan | **FD1: 5G, Wiewless & Components**<br>FD1-1<br>**A 28-GHz 2x2 Antenna Array Integrated with a Butler-matrix Beamformer IC Based on AiP Technology**<br>Wen-Chun Hsiao, Hong-Sheng Huang, Sheng-Chi Hsieh, Chen-Chao Wang, ASE Group / Taiwan<br>FD1-2<br>**Analysis and Optimization of a Compact 1x4 Array Antenna for 5G Application**<br>Hong-Sheng Huang, Wen-Chun Hsiao, Yu-Chang Hsieh, Chia-Ching Chu, Sheng-Chi Hsieh, Chen-Chao Wang, ASE group / Taiwan<br>FD1-3<br>**Evaluation of Effective Permittivity of Multilayer Strip-Line Structure with Air Layers Under Substrate Deformation and Prototype of Deformation Suppression Structure**<br>Ushiyama Taiyo[1], Sasaki Mai[1], Tomioka Sayu[1], Hazemoto Tsuyoshi[1], Ono Satoshi[1], Masui Sho[2], Kojima Takafumi[2], Sakai Takeshi[1], [1]University of Electro-Communication, [2]National Astronomical Observatory Japan / Japan<br>FD1-4<br>**Effects of Magnetic Field Exposure on Emotional Responses in Living Organisms**<br>Daiki Hirabayashi, Yuno Matsuyama, Daisuke Yamada, Akiyoshi Saitoh, Takahiko Yamamoto, Tokyo University of Science / Japan | **FE1: DMR-M-3**<br>FE1-1<br>**High-Speed Ball Shear Mechanism on Ni-Au Substrate & Thermal Aging Effect**<br>Nien-Chun Lin, Hsin-Chih Shih, Ching-I Tsai, Chin-Li Kao, Chen-Chao Wang, C. P. Hung, ASE / Taiwan<br>FE1-2<br>**Study on the Global-Local Method with Critical Mesh Size Control for 3D Wafer-Level Packaging Simulation Time Reduction**<br>C. A. Yang, K. N. Chiang, National Tsing Hua University / Taiwan<br>FE1-3<br>**Advanced Short Defect Repair Techniques for Enhancing Yield in Packaging Architectures**<br>Adam Ginsburg, KLA / Israel<br>FE1-4<br>**Characterization of Signal Variations during the Self-Sharpening Process of Ceramic Diamond Grinding Wheels**<br>Yu-Kun Lin, Feng Chia University / Taiwan |
| 11:50<br>12:40 | **Lunch Time** | | | | |
| 12:40<br>14:20 | **FA2: Die Level Hybrid Bonding Technology**<br>FA2-1 <Session Invited><br>**Die to wafer Hybrid bonding: from challenge to a new Industry standard**<br>Pavel Seroglazov, BESI / Netherlands<br>FA2-2 <Session Invited><br>**Hybrid Bonding for Heterogenous Integration**<br>Viorel Dragoi, Hiroshi Yamamoto, EV Group / Austria<br>FA2-3 <Session Invited><br>**Suss Direct D2W Hybrid Bonding solutions**<br>Muller Philippe, SUSS MicroTec Solutions / Germany | **FB2: Interposer**<br>FB2-1<br>**Multi-Stepped Solder Resist Patterning Technology for Advanced Package**<br>Meiten Koh[1], Yuya Suzuki[2], Yuji Toyoda[3], [1]Taiyo Ink MFG. / Japan, [2]Taiyo America / US, [3]Mitsubishi Paper Mills /Japan<br>FB2-2<br>**Moisture Diffusion Analysis of FOCoS Package During Assembly Processes**<br>Dao-Long Chen, Tang-Yuan Chen, Fan-Yu Min, Wei-Hang Tai, Chen-Hung Lee, Chen-Chao Wang, Chih-Ping Hung, ASE / Taiwan<br>FB2-3<br>**Anti-oxidation for Copper by Galvanic Replacement**<br>Yu-hao Chou, Kun-yuan Zeng, Shih-kang Lin, National Cheng Kung University / Taiwan<br>FB2-4<br>**Adhesion Characteristics of Directly Sputtered Copper Seed Layer on Cycloolefin Polymer Using Atmospheric Pressure Plasma Treatment**<br>Akihiro Shimizu[1,2], [1]Ushio, [2]Gifu University / Japan | **FC2: Advanced Packaging-6**<br>FC2-1<br>**Development of Warpage Control Techniques in Multi-Chip Fan-Out System-in-Package (SiP) Using Redistribution Layer (RDL) Technology**<br>Jr-Wei Peng, Chih-Cheng Hsiao, Chin-Hung Wang, ITRI / Taiwan<br>FC2-2<br>**Advanced Packaging Solutions by Intergrateing 2.5D/3D Chiplet,Wafer Panel Level Package**<br>T. Kubota, S. Hayashiguchi, Y. Kajikawa, S. Teramoto, K Izusawa, TOWA / Japan<br>FC2-3<br>**Cu Pillar Plating Process on Lare Panel Fan-Out for High Performance Computing application**<br>Powei Lu, Ming Tzung Kuo, Jeffrey Yang, Yuan Feng Chiang, Jen Kuang Fang, ASE / Taiwan<br>FC2-4<br>**A novel of UV Curable Wafer Back Side Protection Film**<br>Jun Maeda, Toshiki Inoue, Soki Sato, Shigeyuki Yamashita, LINTEC / Japan | **FD2: Thermal Management-1**<br>FD2-1 <Session Invited><br>**Thermal Resistance Across Semiconductor Interfaces in Electronics**<br>Zhe Cheng, Peking University / China<br>FD2-2<br>**Enhanced performance of high-power density semiconductor chips using CVD diamond heat spreaders**<br>Ian Friel, Element Six / United Kingdom<br>FD2-3<br>**Baking Temperature Optimization for Reducing Interfacial Thermal Resistance in Polymer/SiC Bilayer Structure Using Optical-Interference Contactless Thermometry (OICT)**<br>Jiawen Yu, Hiroaki Hanafusa, Seiichiro Higashi, Hiroshima University / Japan<br>FD2-4<br>**A Fundamental Study on Interfacial Properties of Indium Thermal Interface Materials**<br>Po-hsiang Juan, Kuan-chen Kung, Shih-kang Lin, National Cheng Kung University / Taiwan | **FE2: DMR-M-4**<br>FE2-1<br>**Simulation of CUF Fillet Height and Minimize Void on Reliability**<br>Tzu Chieh Chien[1], Yuan Hung Sun[2], Chao Lin Shih[3], Hui Chung Liu[4], Lu Ming Lai[5], Kuang Hsiung Chen[6], [1]ASE Group / Taiwan<br>FE2-2<br>**Sinusoidal and Random Vibration Analysis of SAC305 Electronic Assemblies Based on Printed Circuit Board Strain**<br>J-B. Libot, P. Milesi, Hooke Electronics / France<br>FE2-3<br>**Thermal Stress-Strain Behavior of Cu on Metallized $Si_3N_4$ Substrate Under Thermal Cycling**<br>Minh Chu Ngo, Hiroyuki Miyazaki, Kiyoshi Hirao, Tatsuki Ohji, Manabu Fukushima, AIST / Japan<br>FE2-4<br>**Optimized Flux-Less Bonding Process for High Throughput Using Simplified Equipment**<br>Kentaro Mihara[1], Takashi Hare[1], Katsumi Terada[1], Toyoharu Terada[1], Chienshuo Huang[2], Yuhao Lo[2], Jun Mizuno[2], [1]Toray Engineering / Japan, [2]National Cheng Kung University / Taiwan |
| 14:20<br>14:30 | **Break** | | | | |
| 14:30<br>16:10 | **FA3: Glass PKG-3**<br>FA3-1<br>**Examination of Panel-Level Manufacturing Methods for Glass Core Substrates**<br>Shun Mitarai, Kiwamu Adachi, Takahiro Igarashi, Kosuke Seki, Naoki Kakoiyama, Yuto Tanaka, Shuichi Oka, Masashi Nakazawa, Hayato Iwamoto, Sony Semiconductor Solutions / Japan<br>FA3-2 <Session Invited><br>**Challenge for Glass Core Substrate with the Stress Analysis and Reliability**<br>Satoru Kuramochi, Dai Nippon Printing / Japan<br>FA3-3 <Session Invited><br>**Multilayer Glass Technology for Advancing Packaging and Substrate Innovation**<br>Akira Tamura, FICT / Japan<br>FA3-4 <Session Invited><br>**Glass PKG Technology Trend & Core Items**<br>Tetsuya Onishi, Grand Joint Technology / Hong Kong | **FB3: Printing Process**<br>FB3-1<br>**Evaluation of Printing Characteristics of Inks Containg Plasmonic Nanoparticles**<br>Akinobu Yamaguchi[1], Toshiya Yasunaga[2], Kyoko Namura[3], Motofumi Suzuki[3], Takao Fukuoka[3,4], [1]Toyo University, [2]Aichi Gakuin University, [3]Kyoto University, [4]Archilys / Japan<br>FB3-2<br>**Silver-Based Metal-Organic Decomposition With 3D Inkjet Printing for Selective Package-Level EMI Shielding**<br>M.-H. Chen, W.-H. Wang, R.-J. Kao, Y.-E. Yeh, ASE / Taiwan<br>FB3-3<br>**Inducing Dynamic Percolation of Stretchable Printed Wires During Three-Dimensional Forming**<br>Rina Aida, Masahiro Inoue, Gunma University / Japan<br>FB3-4<br>**Fine Printing by Gravure Offset Using Low-Temperature Sintered Copper**<br>Shingo Ohshima, Chisato Oyama, Yoshihiro Ohyama, Ikeda Hideki, [1]KOMORI, [2]SERIAI / Japan | **FC3: Advanced Packaging-7**<br>FC3-1<br>**Next Generation Chiplet Technology Development: Focusing on Fine RDL Patterning**<br>M. Sasago[1,6], H. Nishizawa[2,4,6], T. Doi[2,6], M. Ozono[3,6], H. Kimuro[3,6], S. Yamamoto[2,4], K. Suzuki[4], S. Takahashi[5,6], Y. Minami[5,6], M. Yasuda[1,6], Y. Hirai[1,6], T. Saito[1,6], [1]Osaka Metropolitan University, [2]Doi Laboratory, [3]AIST Kyushu, [4]Kyushu Institute of Technology, [5]Lithotech Japan, [6]RCS consortium / Japan<br>FC3-2<br>**Investigation From the Lithography of the Possible of Forming Less Than 8 µm Pitch Required for Advanced Packaging**<br>Yu Abe, Naoya Sohara, Ryotaro Takahashi, Toshimitsu Arai, Hirosuke Takamatsu, Ushio / Japan<br>FC3-3<br>**Approach of Graphic Dynamic Adjustment Integrate to Laser Direct Imaging Solution on 600MM Panel Fan Out**<br>Ping-Ching Shen, Sheng-Feng Huang, Ping-Feng Yang, Jen-Kuang Fang, ASE Group / Taiwan<br>FC3-4<br>**Advanced Post Overlay Compensation for Enhanced Lithography Overlay Accuracy for Next-Generation AICS Packaging**<br>John Chang, Keith Best, Xin Song, Timothy Chang, Onto Innovation / US | **FD3: Thermal Management-2**<br>FD3-1 <Session Invited><br>**Two-Phase In-Situ Thin Liquid Film Cooling for Computing Module With $600W/cm^2$ Heat Flux**<br>Qidong Wang, Institute of Microelectronics of the Chinese Academy of Sciences / China<br>FD3-2<br>**Improvement of Air-Cooling Performance Utilizing Breathing Phenomenon Induced by Corrugated Lotus Copper Fins**<br>R. Kubota[1], K. Yuki[1], K. Yuki[1], T. Ogushi[2], M. Murakami[2], T. Ide[2], [1]Tokyo University of Science, Yamaguchi, [2]Lotus Thermal Solution / Japan<br>FD3-3<br>**Cu/Diamond Composite Heat Spreader for Thermal Management of Advanced Electronic Devices**<br>Masato Sakai, Satoshi Teraji, Tasuku Hamano, Ishihara Chemical / Japan<br>FD3-4<br>**Cancelled** | **FE3: Materials for High Speed Application**<br>FE3-1 <Session Invited><br>**Thin-Film Lithium Niobate based high-speed modulator and future perspective**<br>Rai Kou-Takahashi[1], Toshiya Murai[1], Kazumasa Takabayashi[2], Masahiko Imai, Guangwei Cong[1], Koji Yamada[1], [1]AIST, [2]Fujitsu Optical Components / Japan<br>FE3-2<br>**High-Speed Signal Transmission Fabricated by Silver-Seed Semi Additive Process**<br>Rei Tamura, Akira Murakawa, Norimasa Fukazawa, Wataru Fujikawa, DIC / Japan<br>FE3-3<br>**Material Property Extraction Using Microstrip Antennas for mm-Wave Applications**<br>Tian-Lin Zhang[1], Sung-Mao Wu[2], Bo-Yang Jheng[3], Guan-Yu Hong[4], National University of Kaohsiung / Taiwan |
| 16:10<br>16:30 | **Break** | | | | |

| | Room A | Room B | Room C | Room D | Room E |
|---|---|---|---|---|---|
| 16:30<br><br>18:10 | **FA4: Automation Technology for Wafer/Panel Level Process**<br>**FA4-1 <Session Invited>**<br>**Reimaging and Transforming Package Assembly and Test Manufacturing**<br>Jeffrey S. Pettinato[1,2], [1]Intel / US, [2]SATAS / Japan<br>**FA4-2 <Session Invited>**<br>**Automated Material Handling System (AMHS) as Blood Vessels in a Semiconductor Factory**<br>Kenji Kumagai, Wataru Kitamura, Murata Machinery / Japan<br>**FA4-3 <Session Invited>**<br>**Automation Technology for Wafer/Panel Level Process**<br>Shinichi Nakashima, DAIFUKU / Japan<br>**FA4-4 <Session Invited>**<br>**Automated Material Handling System**<br>Mitsunori Harada, SHARP / Japan<br>**FA4-5 <Session Invited>**<br>**Automatic Transportation AMR(Autonomous Mobile Robot) System For Advanced Back-end Processes**<br>Kazuma Nakaguchi, SINFONIA TECHNOLOGY / Japan | **FB4: Adv. Cu Interconnect Technologies for Chiplets**<br>**FB4-1 <Session invited>**<br>**Chip-let Heterogeneous Integration Packaging Based on Fan-Out Interposer Technology**<br>Jung Won Lee, nepes / Korea<br>**FB4-2<Session invited>**<br>**Advanced Substrate for High Performance AI Computing System**<br>Yu-Hua Chen, Unimicron Technology / Taiwan<br>**FB4-3 <Session invited>**<br>**Integrated Systems Approach from an Equipment Supplier's Perspective in the Advanced Packaging Era**<br>Ji Chul Yang, Hirotaka Satori, EBARA / Japan<br>**FB4-4 <Session invited>**<br>**High-resolution direct-write system for advanced package by unique spatial light modulator**<br>Yuichi Nishimoto SCREEN Holdings / Japan | **FC4: Advanced Packaging-8**<br>**FC4-1**<br>**Reliability and Warpage of High Density Package Using Organic Interposer for Heterogeneous Integration**<br>Yoshihiro Kobayashi, Shota Miki, Shinko Electric industries / Japan<br>**FC4-2**<br>**RDL Formation Using Low Df Thermosetting Film (Progress of the Chiplet Integration Platform Consortium in Japan)**<br>Yusuke Naka[1], Meiten Koh[1], Yoichiro Kurita[2], Ichiro Kono[3], Yasuhiro Morikawa[4], Takafumi Fukushima[5], [1]Taiyo Ink MFG., [2]Institute of Science Tokyo, [3]AOI Electronics, [4]ULVAC, [5]Tohoku University / Japan<br>**FC4-3**<br>**Surface Modification for PI-to-PI Direct Bonding**<br>Yu-Kuang Chen, Chang-Ju Hsu, Jenn-Ming Song, National Chung Hsing University / Taiwan<br>**FC4-4**<br>**Advancements in Advanced IC Substrate Packaging: Systek ETS 1200 for Enhanced Performance and Sustainability**<br>Saminda Dharmarathna[1], Fengqi Zhang[1], Maddux Sy[3], Charles Bae[2], Brian Gokey[1], Ernie Long[1], [1]MacDermidAlpha Electronics Solutions / USA, [2]MacDermidAlpha Electronics Solutions / Korea, [3]MacDermidAlpha Electronics Solutions / Taiwan | **FD4: Thermal Management-3**<br>**FD4-1 <Session invited>**<br>**Thermal Test Vehicles for Characterization of the Thermal Performance for Large Silicon Chips**<br>Dongkai Shangguan[1], Cheng Yang[2], Yin Hang[3], [1]Thermal Engineering Associates / US, [2]STATS ChipPAC / Singapore, [3]Meta Platform / US<br>**FD4-2**<br>**Power Devices Sandwiched Between Silver-Diamond Parts for High Performance Power Modules**<br>R. Khazaka[1], A. Casado Ramoneda[1,2], Y. Avenas[2], T. Youssef[1], C. Gautier[1], S. Azzopardi[1], T. Murakami[3], M. Tamaru[3], [1]Safran SA, [2]Université Grenoble Alpes / France, [3]TECNISCO / Japan<br>**FD4-3**<br>**Thermal Transfer Analysis by Phonon Vibrations at Interface Between Filler and Resin in Thermal Interface Material**<br>Osamu Arao, Masashi Kitsunezuka, Akira Shintai, DENSO / Japan<br>**FD4-4**<br>**Verification of Differences in Thermal Resistance of Cascode Device Packages Due to Heating Power Ratio of Heat Sources**<br>Aiko Shimada, Wasanthamala Badalawa, Yoshitaka Aoki, Tomoaki Hara, Siemens / Japan | |

# ■ Poster Session

Poster sessions will be held from 15:50-16:50 on April 16 and from 17:40-18:40 on April 17.

**P01** Optimization of PVD SiCN Deposition for Cu/SiCN Hybrid Bonding Applications
Junyoung Choi, Suin Jang, Dongmyeong Lee, Hoogwan Lee, Sarah Eunkyung Kim, Seoul National University of Science and Technology / Korea

**P02** Exploring the Potential of Fly Cutting for Polymer Planarization in Cu/PDMS Hybrid Bonding
Suin Jang, Junyoung Choi, Dongmyeong Lee, Hoogwan Lee, Sarah Eunkyung Kim, Seoul National University of Science and Technology / Korea

**P03** Effect of Noble Metal Passivation Deposited by ECD on Cu Surface for Low-Temperature Cu-to-Cu Bonding
Dongmyeong Lee, Junyoung Choi, Suin Jang, Hoogwan Lee, Sarah Eunkyung Kim, Seoul National University of Science and Technology / Korea

**P04** Advanced Package Solution Applied on High Performance Computing for Heterogeneous Integration
Chen Chao Wang, Chih Yi Huang, Hung Chun Kuo, Ming Fong Jhong, Fu Chen Chu, Chung Hung Lai, Hung Hsien Huang, Lee Hsu Yang, Chih Pin Hung, ASE Group / Taiwan

**P05** Study of Low Temperature Cu-to-Cu Bonding using Reducing Plasma Pretreatment
Hoogwan Lee, Dongmyeong Lee, Junyoung Choi, Suin Jang, Sarah Eunkyung Kim, Seoul National University of Science and Technology / Korea

**P06** Low-Temperature Femtosecond Laser Processing for Enhanced Via Hole Morphology in Semiconductor Packaging
Taesik Kim[1,2], Jaebeom Lee[1,2], Seon-Jin Choi[2], Jiyong Park[1,3], [1]KITECH, [2]Hanyang University, [3]Korea National University of Science and Technology / Korea

**P07** Heterogeneous Integration of Magnetic Spin Wave and CMOS Chips into a Hybrid Computing System
Christian Voigt[1,2], Martin Hempel[2], Ruben Kahle[2], [1]Technical University of Berlin, [2]Fraunhofer IZM / Germany

**P08** Signal Integrity Enhancement of Die-to-Die Interconnection by Using a Vertically Asymmetric Pattern
Jaewon Lee[1,2], Kihun Ok[1], SoYoung Kim[1], [1]Sungkyunkwan University, [2]Samsung Electronics / Korea

**P09** Simulation of Signal Integration and Power Integration in Advanced Packaging Circuit Design
Shu-Chin Huang, Sung-Mao Wu, National University of Kaohsiung / Taiwan

**P10** Analysis of Parasitic Effects in Packaging With RDL
Jyun-yu Chen, Sung-Mao Wu, Shin-Shian Wu, National University of Kaohsiung / Taiwan

**P11** Parametric Investigation of Surface Morphology in Through-Glass Vias (TGVs) Fabricated via Femtosecond Laser Processing
Jaebeom Lee[1,2], Taesik Kim[1,2], Seung Hwan Lee[2], Jiyong Park[1,3], [1]KITECH, [2]Hanyang University, [3]Korea National University of Science and Technology / Korea

**P12** Cu Metallized Glass Core Evaluation & Testing Method
T. Onishi[1,2], A. Okitmoto[1], K. Inoue[1], T. Watanabe[1], M. Takayama[1], [1]Koto Electric / Japan, [2]Grand Joint Technology / Hong Kong

**P13** Within-Wafer and Within-Die Uniformity of Bond Strength for Hybrid Bonding
Daiki Kobayashi[1], Junya Fuse[1], Yusuke Kondo[1], Yuki Yoshihara[1], Marie Sano[1,2], Fumihiro Inoue[1], [1]Yokohama National University, [2]Kanagawa Institute of Industrial Science and Technology / Japan

**P14** Implementation of Double-Side Calibration and Measurement for Q-Band 50GHZ Application
Chia-Chu Lai1, Sam Lin, Vito Lin, Andrew Kang, Yu-Po Wang, Siliconware Precision Industries / Taiwan

**P15** The Application of Electric Feed-in With the Low Sensitivity and Low Spatial Resolution Probe
Yu-Kai Kuo, Guan-Yu Hong, Tsai-Feng Wu, Shin-Shian Wu, Yu-Zhi Ma, Sung-Mao Wu, National University of Kaohsiung / Taiwan

**P16** Efforts to Improve the Accuracy of Simulation Technology for Package Substrates by Acquiring Realistic Material Properties
Satoshi Nakamura, Aki Tanaka, Kyocera / Japan

**P17** Monopole and Loop Feed-In Substrate Integrated Waveguide Splitter Design
Yi-Chang Tsai, Sung-Mao Wu, National University of Kaohsiung / Taiwan

**P18** Design and Experimental Verification of Electric Near Field Probe
Bing-Wei Chen, Sung-Mao Wu, National University of Kaohsiung / Taiwan

**P19** Process-Oriented Simulation and Warpage Mitigation Strategies for Fan-Out Package-on-Package (FOPoP) Technologies
Mei-Ling Wu, Jin-Yu Wu, National Sun Yat-sen University / Taiwan

**P20** Blue Microfluidic Electrogenerated Chemiluminescence Cell Using a Fluorescent Emitter and a Redox Mediator
Ayari Tobori[1], Sara Yamaguchi[1], Ryoichi Ishimatsu[2], Takashi Kasahara[1], [1]Hosei University, [2]University of Fukui / Japan

**P21** Adhesion of Si and Lithium Niobate via Perhydropolysilazane for Photonic Substrate Fabrication
Kei Hishinuma, Kai Takeuchi, Eiji Higurashi, Tohoku University / Japan

**P22** Indium Through Si Via for Quantum Chiplet Integration
Yugi Otake[1], Mai Thi Ngoc La[1], Kenta Hayama[1], Jowesh Avisheik Goundar[1], Fumihiro Inoue[1,2], [1]Yokohama National University, [2]Semiconductor and Quantum Integrated Electronics Research Center / Japan

**P23** High-Precision Thin-Film Bending Sensor with Fully Sliding Packaging Structure for Robotic Surgical Endoscope
Hao Liu[1], Michitaka Yamamoto[1], Toshihiro Itoh[1], Seiichi Takamatsu[2], [1]The University of Tokyo / Japan, [2]State University of New York at Binghamton / US

**P24** High-Speed Signal Transmission Comparative Analysis of Huray and Groisse Models for Copper Foil Surface Roughness
Yu-Zhi Ma[1], Shin-Shian Wu[1], Lung-Shu Huang[2], Tsai-Feng Wu[1], Sung-Mao Wu[1], [1]National University of Kaohsiung / Taiwan, [2]Innolux / Taiwan

**P25** A Simple Method of Dielectric Constant Measurement Using a Microstrip Resonator
Hiroki Matsuura, Koji Wada, The University of Electro-Communications / Japan

**P26** Surface Treatment for Wafer Bonding Using Atmospheric Water Vapor Plasma Technology
Wonyoung Choi, Bumki Moon, Seung ho Hahn, Youngjoo Lee, Byeongtak Park, Jungshin Lee, Kyeongbin Lim, Samsung Electronics / Korea

**P27** A Mild Surface Activation using Vacuum Ultraviolet Irradiation Under Redox Gases for Semiconductor Bonding Materials
S. Endo, A. Shimizu, Ushio / Japan

**P28** Optimization of Au-Ag-Pd Alloy Wire Bonding for Stacked NAND Flashes
Min-Chen Huang[1], Ruenn-Bo Tsai[1], Jin-Bao Wang[2], Chao-Yung Wang[2], Tsung-Jen Kang[2], [1]National Sun Yat-sen University, [2]Orient Semiconductor Electronics / Taiwan

**P29** Development Fine Pitch Organic Hybrid Bonding Application
Chih-Jing Hsu[1], Che-Ming Hsu[1], Min-Tzu Hsu[1], Hsu-Nan Fang[1], Yuan-Feng Chiang[1], Jen-Chieh Kao[1], Yung-I Yeh[1], Kazuaki Ebisawa[2], Makiko Irie[2], [1]ASE Group / Taiwan, [2]Tokyo Ohka Kogyo / Japan

**P30** A Transceiver IC Development for Wired Data Communication Using Mode Division Multiplex Transmission Method
Ryoma Sakida[1], Hayato Yatabe[2], Yuki Fukumoto[2], Tohlu Matsushima[2], Takefumi Yoshikawa[1], [1]Toyama Prefectural University, [2]Kyushu Institute of Technology / Japan

**P31** The Post Mold Cure Effect on the Microstructural and Mechanical Properties of Ag and Cu Joints
ByeongChan Kim[1], YehRi Kim[1,2], Dongjin Kim[1], [1]KITECH, [2]Korea University / Korea

**P32** Application of Indium Sheet Thermal Interface Material in Advanced Semiconductor Packaging
Wen-Yu Teng, Debby Li, Jackson Lee, Liang Yih Hung, Andrew Kang, Don Son Jiang, Yu-Po Wang, SPIL / Taiwan

**P33** Preparation of Fluorine-Free, Transparent, Hydrophobic Coatings as Protectors for Electronic Packaging
Chih-Feng Wang[1], Meng-Hang Tsai[1], Sheng-Hsiang Hsu[2], [1]National Sun Yat-sen University, [2]ASE / Taiwan

**P34** Evaluation of the Oxidation Resistance of Cross-Linked Gelatin-Coated Copper Particles
Tatsuya Yamaguchi, Hiroki Tsukamoto, Tetsu Yonezawa, Hokkaido University / Japan

**P35** Characterization of Chitin or Chitosan/PCL Nanofibers Prepared by Electrospinning
K. H. Wu, C. Y. Wu, C. L. Chung, I-SHOU University / Taiwan

**P36** PFAS-Free Assembly Material Development
Wei-Chun Chen, Han-Gung Chen, Fenny Liu, Liang-Yih Hung, Andrew Kang, Yu-Po Wang, Siliconware Precision Industries / Taiwan

**P37** Preparation of $UCr_4C_4$ -Type Fluorescent Fiber $(Na_{1-x-y}K_xLi_y)_{1-z}[Li_3SiO_4]:zEu^{2+}$ by to Change the Ratio of K and Li by Electrospinning
J. Y. Shih, Y. J. Zhu, C. L. Chung, J. D. Lin, I-SHOU University / Taiwan

**P38** Mechanical Properties Characterization of Silicon Carbide Coated Graphite Composites for MOCVD Structural Design
Kuo-Shen Chen, HsuaN-Ting Huang, Wu-Jun Liu, Tzu-En Liu, National Cheng-Kung University / Taiwan

**P39** Interfacial Reactions in Sn/Ag/Cu Sandwiched Structure
Yu-Xuan Yang, Chih-Ming Chen, National Chung Hsing University / Taiwan

**P40** Development of Indium-Based Low Temperature Solder Alloys Under Martian Conditions: Overview
Jiye Zhou[1], Xin F. Tan[1], Stuart D. McDonald[1], Tetsuro Nishimura[2], Kazuhiro Nogita[1], [1]The University of Queensland / Australia, [2]Nihon Superior / Japan

**P41** Basic Investigation to Simplify the Prototype of Fat-Equivalent Electromagnetic Phantom for Microwave Mammography
Kotomi Inada, Takahiko Yamamoto, Tokyo University of Science / Japan

**P42** Effects of Current Mode and Electrodes on the Properties of Electroplated Fe-Ni Invar Alloy
Na-Young Kang, Jae-Ho Lee, Hongik University / Korea

**P43** Surface Treatment of AlN Filler for Improvement of Reliability in Silicone Resin Composites
M. Takakusaki, I. Masada, Y. Iizuka, T. Hamasaka, A. Sakamoto, G. Hamasaka, Tokuyama / Japan

**P44** Estimation of Adhesive Strength and Thermal Cycling Lifetime with Molecular Dynamics Simulation and Finite-Element Analysis for Sintered Cu and Sintered Ag
Dai Ishikawa[1], Hideo Nakako[1], Thomas Blank[2], Felix Steiner[2], [1]Resonac / Japan, [2]Karlsruhe Institute of Technology / Germany

**P45** Silver Paste Transferability During Imprinting Using PDMS Replica Mold
H. Komatsu, D. Sakai, N. Shimoishizaka, CONNECTEC JAPAN / Japan

**P46** Solid-State Mg Heat Sink Direct Cooling Bonding with Refill Friction Stir Spot Bonding for Power Inverters
Shihun Park[1], Shin-Il Kim[1], YehRi Kim[1], Seungyeop Baek[2], Dongjin Kim[1], [1]KITECH, [2]Korea Automotive Technology Institute / Korea

**P47** Research on System Circuit Thermal-Electric Analysis Based on Non-contact Near-Field Measurement
Cheng Hsuan Liu[1,2], Sung Mao Wu[1,2], [1]Micro Electronic Packaging Laboratory, [2]National University of Kaohsiung / Taiwan

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