

# Call for Papers

# ICEP-IAAC 2018

2018 International Conference on Electronics Packaging  
and IMAPS All Asia Conference

April 17-21, 2018

Hotel Hanamizuki, Kuwana, Mie, Japan

Sponsored by JIEP, IEEE CPMT Society Japan Chapter and IMAPS

## Major Topics

### Advanced Packaging

2.5D/3D, Advanced CSP and POP, Advanced Flip-Chip, Automotive, Embedded and Advanced Substrates, Fan-Out, Heterogeneous Integration and SiP, High Performance Computing and Data Center, Interposers, Temporary Bonding/De-Bonding, TSV/TGV, Wafer Level & Panel Level Process, Wafer Level Packaging, Wearable & IoT, Wireless Interconnection

### Design, Modeling, and Reliability

Advanced Package Reliability (TSV/TGV, 2.5D/3D Packaging, WCSP, Fan-Out, Embedded Technologies), Automotive Reliability Requirements, Challenges in SiP Reliability, Drop and Dynamic Mechanical Reliability, Failure Analysis Techniques and Materials Characterization, Fracture and Warpage in Packages, High Voltage Packaging and IoT Reliability, High-Speed Board Design, Interconnect Reliability (Flip-Chip, Wire-Bond), Mechanical Design and Reliability, Physics of Failure, Probabilistic Design for Reliability (PdFR), Reliability Test Methods and Life Models, Signal and Power Integrity, System Level Reliability (Testing, Modeling), TCAD

### Emerging Technologies

3D Printing, Anti-Counterfeiting, Bendable electronics, Biomimetics, Biosensors, Compact & Autonomous Sensor Packaging, Components for Internet of Things (IoT) and Smart Electronics, Device Applications, Disposable/Dissolvable Packaging, Flexible electronics, Future diagnostic and treatment solutions, Hearing aids, Heterogeneous Integration, Implantable defibrillators, Implantable Device Packaging, Inkjet, Interventional catheters, Materials and Approaches to Interconnects and Packaging, Medical Electronics, Micro opto electro mechanical systems (MOEMS), Microelectromechanical systems (MEMS), Microfluidics, Nano Imprint, Nano-Battery, Nanoelectromechanical systems (NEMS), Neurostimulator and drug delivery, New Additive Packaging Process Technologies and Materials, New Materials and Methods for Packaging Microfluidics, Novel Substrates, Organic Semiconductors, Packaging for Wireless, Photovoltaic, Pillcams, Redundancy, Repair, Security, Self-Alignment and Assembly, Self-Healing, Sensor Devices, Stretchable electronics, Structural Electronics, Ultrasound transducers, Wafer Level Integrated Silicon Photonics, Wearable Electronics, Wireless communications

### High-Speed, Wireless & Components

3D Printed RF Components and Modules, 5G, Advanced Components (Materials, Structures), Ambient Intelligence, Antennas, Automotive Sensors, Beamforming, Design and Analysis of Power Delivery Systems, Electrical Modeling and Design, EMI, Fabrication and Characterization, Filters, Flexible Electronics, Full Duplex, High-Speed, High-Speed Data Transfer/Communications, High-Speed Systems (Design, Analysis), Imagers, Integrated Voltage Regulators (IVR), LTE, M2M Platforms, Massive MIMO, Microwave, Millimeter Wave, Mixed-Signal, mm Wave and THz T/R Modules, Modules & Sub-Systems, Power and Signal Integrity, Power Management, Proximity Sensors, Radars, RF, RF to THz Devices & Passive Components, RFID and Tagging, RF-MEMS, RF-Opto, Small Cell, Wearable and Sensor Technologies for Internet of Things (IoT), Wireless Power, Wireless Sensor and Computing Nodes, WLAN

### Interconnections

2.5D/3D, Automotive, Conductive Adhesives, Embedded Multi-die Interconnect Bridge, Embedded Systems, Energy Harvesting, Fan-Out and Fan-In, Flip-Chip (Bonding, Materials, Reliability), Harsh Environments, IMC Interconnect, Interconnects for Bio-Medical, RDL, Si/Glass/Organic Interposers, Solder Bumping and Cu Pillar, Thermal/Mechanical/Electrical Tests & Reliability, TSV/TGV (Fabrication, Characterization, Reliability), Wafer Level & Panel Level Interconnects, Wearables, Wirebonds (Process, Reliability), WLCSF

### Materials and Processes

3D Materials & Processing, 3D Materials and Processing, Advanced Assembly Technology Solutions, Advancement in 3D Handling & Packages, Advances in RF Materials & Components, Battery Materials, Carbon Electronics, Dicing and Singulation, Embedded/Hybrid Package Manufacturing Process, Emerging Electronic Materials, Enhancement in Thermal Compression Bonding Processes, Flexible and Wearable Electronics, Healthcare/Fitness Component Assembly, Large/Ultra Large Package (SiP, SIM, MCP) Integration and Processing, Next Generation Packaging Substrates, Next Generation Substrates for Package Integration, Novel Assembly Technologies, Novel Fan-Out Interconnections, Novel Interconnect Materials, Optoelectronic Materials, Panel Level Manufacturing for WLP, Panel Processing & Materials, Performance Enhanced Materials (Adhesives, Underfills, TIMs, Dielectrics, Molding Compounds, Solder, Temporary Bond), Performance Enhanced Materials (Prepregs, Plating solution, Photoresist), Performance Enhanced Printing Wiring Board (Fine line, Low CTE, Coreless, Thin Core), Thin Die/Thin Mold/Thin Package Handling and Assembly, Via Formation and Filling, Wafer Level Packaging, Warpage Control/Management in Board Level Assembly, Wearable/IoT Package Assembly

### Optoelectronics

3D Photonics, Advanced Optical Connectors, High-Efficiency LEDs and High Power Lasers, Integrated Optical Sensors, Integrated Photonics Modules, Materials and Manufacturing Technology, Mid-Board/On-Board Optical Modules, Optical Chip-Scale and Heterogeneous Integration, Optical Interconnects, Optical Printed Circuit Board, Optical Waveguide Circuits, Optoelectronic Assembly and Reliability, Transceivers and Silicon Photonic Modules

### Power Electronics Integration

AC-DC Converters, Capacitors / Supercapacitors, DC-DC Converters, Devices and Components, Fast Recovery Diodes, GaN HEMTs, Hybrid System, Interconnects and Fuses, Inverters/converters for electric vehicles, Lamp Ballasts and LED Lighting, Magnetic materials and components, Mechatronic Integration, Motor Drives and Inverters, Packaging of high-temperature power electronics, Power Electronics for Utility Interface, Power Module, Power Silicon MOSFETs / BJTs / IGBTs, Sensors, SiC MOSFETs and BJTs, Systems and Components Reliability, Ultra High Power Density Integration

### Thermal Management

Advanced Cooling Modules, Fans and Blowers, Heat Pipes, Heat Sinks, Micro and Nano Scale Heat Transfer, Thermal Issues in Devices, Thermal Measurements

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## Abstract Deadline and Paper Submission

### Important dates

Abstract submission open: **August 1, 2017**

Abstract deadline: **October 31, 2017**

Notification of acceptance: **December 13, 2017**

Final manuscript deadline: **February 16, 2018**

Please submit your abstract (2pages) using the template available at the conference website. <http://www.jiep.or.jp/icep/>

Accepted and presented papers will be published in the conference proceedings and submitted to IEEE Xplore as well as other Abstracting and Indexing (A&I) databases (EI Compendex and INSPEC).

## About ICEP

ICEP is the largest international conference on electronic packaging in Japan, attracting more than 360 attendees and hosting about 35 technical sessions. ICEP provides a strong platform to demonstrate your technologies and products as well as expand your customer network. It is jointly sponsored by JIEP, IEEE CPMT (Components, Packaging, and Manufacturing Technology) Society Japan Chapter, and iMAPS. The conference has technical sessions covering a wide range of topics including advanced packaging, design, modeling and reliability, emerging technologies, high-speed, wireless & components, interconnections, materials and processes, optoelectronics, power electronics integration, thermal management.

Since its inauguration in 2001, ICEP has developed into a highly reputed electronics packaging conference in Japan, attended by world-renowned experts in all aspects related to packaging technologies from all over the world.

## Technical Outstanding Paper Awards

Technical outstanding paper are selected for special recognition by JIEP. These awards will be given to the presenter and the co-authors of the technical outstanding papers.

**Eligibility:** The presenter must be listed as are author. Full papers (4-6 pages in conference format) must be submitted on or before the due date.

## Registration Fees

Member of JIEP / IEEE / IMAPS: 41,000 JPY (including reception and the proceedings)

Non Member: 55,000 JPY (including reception and the proceedings)

Students: 12,000 JPY (including the proceedings)

## IEEE CPMT Japan Chapter Young Awards

Award winners are selected for special recognition by IEEE CPMT Society Japan Chapter.

These awards will be given to young scientists and engineers of the excellent papers. IEEE CPMT Society Japan Chapter is sponsoring the awards for excellent paper submitted and presented by young scientists and the engineers at ICEP.

**Eligibility:** Young scientists and engineers must be the lead author and present the paper at the ICEP-IAAC 2018. Presenters who are younger than 35 years old on December 31 of the presentation year are qualified for nomination. The award recipient must be a member of IEEE and CPMT at the time the award is received. Full papers (4-6 pages in conference format) must be submitted on or before the due date.

## Organizing Committee

General Chair: Y. Nogami, Toray Engineering

General Vice Chairs: O. Suzuki, Namics; H. Hirata, Toray Engineering; Y. Taira, Keio University

## Sponsorship Opportunity

We invite you to be an official conference sponsor, which entitles your company to be exposed to the attendees in and outside the conference rooms. The sponsorship for ICEP-IAAC 2018 ranges from 400,000 yen to 30,000 yen. As a sponsor, your company's name and logo will be published in the conference official program, and will appear on the ICEP web site as well as various conference banners. Furthermore, a tabletop exhibition booth is available for the diamond, platinum and gold sponsors to demonstrate and promote your products/services. Please contact the conference secretary for details.

## JIEP Poster Awards

Award winners are selected for special recognition by JIEP.

These awards will be given to the presenter and the co-authors of excellent posters.

**Eligibility:** The presenter must be listed as are author. Full papers (4-6 pages in conference format) must be submitted on or before the due date.

## Contact

Secretary, ICEP-IAAC 2018

JIEP (The Japan Institute of Electronics Packaging)

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## New Global Student Session

We believe the Global student session will be a wonderful opportunity for students to have a presentation of their research results and discussion. By exchanging opinions with overseas students, we expect to innovate motivation of their effort. It's time to invent yourself!

The presenter must be a full-time student for at least one semester after the conference conclusion. The student must be the lead author and present the paper at the ICEP-IAAC 2018.



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