Introduction

A 3D IC is fabricated by stacking dies with Through Silicon Vias (TSVs), bonding wires and/or solder bumps.[1] The dies in the IC were fully tested before the stacking. Thus, it can be assumed that a 3D IC is made of known good dies (KGDs).

Short and open defects can occur at interconnects between KGDs inside a 3D IC in the stacking.[1, 2] Thus, only the interconnects need be tested in the production tests. In this paper, we discuss how to detect defects occurring at interconnects between dies inside a 3D IC.

3D IC testing is classified into 2 types: pre-bond and post-bond testing.[3] Post-bonding testing is discussed in this paper.

Interconnects between an IC and a printed circuit board (PCB) have been tested by boundary scan testing.[4] Similarly, interconnects in a 3D IC can be tested by boundary scan testing.[1] Thus, IEEE 1149.1 test architecture is introduced in dies inside many 3D ICs.

Short defects will generate logical errors by providing complement logic values to the defective interconnects. Thus, short defects between interconnects in a 3D IC are easy to detect using boundary scan testing. Since there are many TSVs inside a 3D IC, boundary scan testing takes a long time. Thus, various kinds of Design for Testability (DfT) methods and built-in test methods have been proposed so as to shorten the test time.[3, 5–8]

On the other hand, open defects at interconnects are more difficult to detect than shorts, since the voltage at a floating interconnect caused by an open defect depends on various kinds of factors. For example, it depends on the layout and logic signals of the neighboring interconnects.[9] Thus, it is very difficult to generate test vectors with which open defects can be detected by boundary scan testing. Also, it takes a long time to locate the defective interconnects. This makes the development of methods to improve yields of 3D ICs difficult. Since open defects at interconnects between dies are difficult to detect, we select them as our targeted defects.

Open defects can be classified into “hard open defects” and “soft open defects.” In a hard open defect, an interconnect is completely divided into two parts but they are not connected to each other. In the case of a soft open defect, the parts are incompletely connected with each other electrically. A soft open defect may be called a “weak open defect.”[2] The defect may be caused by a void or a crack in a TSV.[10]

Open defects that generate logical errors can be detected by boundary scan techniques. However, soft open defects that generate timing error may not be detected by test methods based on boundary scan techniques. They can be detected by electrical testing. Thus, some kinds of electrical test methods have been proposed. The test method proposed in[11] is based on the principle of oscil-
lation testing in analog circuits. Also, an electrical test method with an on-chip sense amplifier has been proposed.[12]

In order to realize high yields of 3D ICs, defective interconnects should be located. Thus, a test method has been proposed based on X-ray computed tomography.[13] It takes a long time to judge whether a soft open defect occurs in an interconnect by the test method. Since there are many interconnects in a 3D IC, we should develop a test method with which a defective interconnect can be located quickly.

Soft open defects will reduce the reliability of an IC. They will result in some increase of propagation delay time. They will grow and can change into hard open defects. Since a hard open defect may generate a logical error[9] and also a timing error, a soft open defect should be detected before it becomes a hard one. Thus, we have proposed an electrical test method with which both hard and soft open defects can be detected.[14] The test method requires us to design ESD input protection circuits inside a die to be tested by the test method. We have prototyped ICs embedding the ESD input protection circuits and shown feasibility of the test experimentally.

The test method proposed in[14] is based on the supply current of the targeted IC. Current probes may be necessary to measure the supply current in the tests. This may result in an expensive test setup. It is important to develop inexpensive test setup. Also, IC designers may be reluctant to modify ESD input protection circuits so as to allow testing by the new method. Thus, we attempted to develop an electrical test method with which 3D ICs can be tested without current probes and a new testable design method for the test method. We examined the feasibility of our electrical testing experimentally and by SPICE simulation.

In this paper, we introduce our new test method and testable design method. Also, we denote the results of our feasibility analysis on our testing.

2. Our Electrical Test Method

Generally, IEEE 1149.1 test architecture is introduced in each of the dies inside a 3D IC so that interconnects between KGDs can be tested easily. This is utilized in our tests.

A logic signal from a TSV is propagated to more than one TSV in memory ICs. However, a logic signal from a TSV is provided to another TSV in many ICs other than memory ICs. Thus, a 3D IC in which each TSV is connected only to one other TSV is targeted in this paper.

An example of our targeted 3D IC is shown in Fig. 1(a). The IC is made of 2 dies, Die#1 and Die#2, that are connected with TSVs. 3D ICs are targeted in our tests in which the dies are connected with bonding wires and/or solder bumps besides the one shown in Fig. 1(a).

We assume that dies in a targeted 3D IC are KGDs. Only open defects in interconnects between dies are targeted in our tests.

A test circuit to detect open defects at interconnects between Die#1 and Die#2 is shown in Fig. 1(b). The interconnects are tested by measuring the voltage across a resistor, $R_c$.

The ESD input protection circuits inside the dies are designed for current to flow in our tests. Modification of the ESD input protection circuits may not be accepted by IC designers, since ESD input protection circuit design is sensitive to the IC process used. Thus, we do not modify the ESD input protection circuits and only add two diodes, $D_{a}$ and $D_{b}$, in front of the input protection circuit as shown in Fig. 2.

When our testable IC is not tested by our test method, the cathodes of $D_{b}$ in the input circuits are connected to the source voltage, $V_{DD0}$. They are connected to GND through $R_C$ only when the IC is tested by our test method.
For example, when the interconnects between Die#i and Die#i+1 in Fig. 2 are tested by our test method, the switch, Swt#1, is connected to the resistor Rc. Also, a high-level signal is provided only to the targeted interconnect and a low-level signal to those with the IEEE 1149.1 test architecture.

Rc is used to reduce IrC in our tests. If Rc is not included, a large IrC will flow and the device under test (DUT) may be destroyed in our tests.

When a defect-free IC is tested by our method, a quiescent current, IrC, flows only through the interconnect in the 3D IC. An interconnect to which a high-level signal is provided is a targeted one. When an open defect occurs at the interconnect, a smaller IrC will be measured than for the defect-free ICs. Thus, it will be detected by (1).

In our tests, a high-level signal is provided to only one interconnect and IrC flows only through the interconnect in the 3D IC. An interconnect to which a high-level signal is provided is a targeted one. When an open defect occurs at the interconnect, a smaller IrC will be measured than for the defect-free ICs. Thus, by monitoring IrC during our tests, it can be specified which interconnect a high-level signal is provided to when (1) is satisfied.

The IC can be tested by boundary scan testing and work in the normal mode with Swt#1 connected to the voltage source VDD0.

Interconnects between the input terminals of the IC in Fig. 1 and input ports of Die#1 will be tested in the same manner as in Fig. 2 by providing our test vectors to Die#1 from a tester. Also, the interconnects between the output terminals of the IC in Fig. 1 and the output ports of Die#2 will be tested by outputting our test vectors from Die#2.

A low-resistance Rc can shorten the time for IrC to become constant. This leads to a high-speed test. However, a small Rc allows a large IrC to flow into the IC. Die#i and Die#i+1 may be broken by the large IrC. Thus, Rc is specified from the maximum value in the permissible range of IrC.

3. Evaluation of Our Electrical Testing

3.1 Evaluation by SPICE simulation

In order to evaluate the feasibility of our electrical tests, we designed a die layout with the 0.18 μm CMOS process of Rohm Co. Ltd., and prototyped an IC that was designed using our testable design method.

We extracted the layout of a circuit block consisting of the followings from the IC: a core circuit, ESD input protection circuit, and boundary scan FF.
tection circuits, and an output protection circuit. We designed the layout of the circuit shown in Fig. 3 from the extracted layout. The layout of Die#1 is the same as Die#2. We converted the layout shown in Fig. 3 into a SPICE net list with an extraction tool, “Caliber,” produced by Mentor Graphics.

ESD input protection circuits should be designed for $I_{OC}$ to flow in our electrical testing. Our designed ESD input protection circuits are shown in Fig. 4. As shown in Fig. 4, diodes in the protection circuit shown in Fig. 2 are made of MOSs. Diodes $D_{sa}$ and $D_{a}$ in Fig. 2 are made of a PMOS of type $M_{pa}$ that is identical to the one of type $M_{pa}$ and a NMOS of type $M_{na}$ that is identical to the one of type $M_{na}$, respectively. The numbers of PMOSs of types $M_{pa}$ and $M_{na}$ are 3 and 7, respectively, in each of our designed ESD protection circuits.

We coded a SPICE net list of the circuit in Fig. 5 with the converted net list of the layout shown in Fig. 3. A SPICE simulation circuit is built by adding a parasitic resistor, $R_p$, and a parasitic capacitor, $C_p$, of a TSV to each interconnect. $R_p = 4 \, \Omega$ and $C_p = 3pF$ are used in our simulation. The resistance of the $R_C$ used in our simulation is 100 $\Omega$.

We inserted an open defect at $S_1$ by adding a resistor, $R_f$, of 100 G$\Omega$ to the coded net list in order to examine the testability of a hard open defect. Also, we inserted a soft open defect which is modeled as resistor $R_f$. In our circuit simulation, $R_f = 100 \, \Omega$ and $R_f = 1 \, k\Omega$ are inserted into the $S_1$, with which additional delays of 288 psec and 2.63 nsec are generated, respectively. The following are used as source voltages as specified by the CMOS process used in our layout design: $V_{DD0} = 3.3 \, V$, $V_{DD1} = 1.8 \, V$.

Test vectors in our evaluations are shown in Fig. 6. In order to examine the test speed of our test method, the test vectors are provided to the circuit per the following time of $T_s$: 1 $\mu$s, 10 nsec and 1 nsec.

Our simulation results are shown in Fig. 7, Fig. 8, and Fig. 9. As shown in these figures, the hard open defect and the soft ones at $S_1$ are detected by our test method, since a
smaller $V_{RC}$ appears than the defect-free circuit when $S_1 = H$. Also, Fig. 9 shows that the defects are detected at a test speed of 1 GHz.

In our ESD input protection circuit, diodes $D_{ia}$ and $D_{ib}$ are added to a typical input protection circuit for open defects at the interconnects between the dies to be tested. The diodes will generate some additional propagation delay. Thus, we examined the delay time. The propagation delay time in our ESD protection circuit is 40 psec as shown in Fig. 10. On the other hand, the time in a general ESD protection circuit is 36 psec, as shown in Fig. 11. Thus, the additional propagation time is 4 psec. We think that speed degradation caused by introducing our testable design is very small.

3.2 Evaluation with a Prototype IC

In a 3D IC, it may be impossible to test the interconnects between dies at the same test speed as in the SPICE simulation results shown in Fig. 9, since the test speed depends on the measurement environment used in the test. The testability of our method should be evaluated by experiments in which real ICs are used.

We examined the testability of our electrical tests in a circuit implemented on a PCB with our prototype QFP-type IC. Only the dynamic change of $V_{RC}$ in the PCB circuit is slower than in a 3D IC. However, the quiescent $V_{RC}$ is used as a test in our method. Also, open defects are easily inserted into a targeted circuit. Thus, we used a PCB circuit to evaluate the testability of our method.
Our experimental circuit is shown in Fig. 12. IC#3 is our prototype IC which was designed by our testable design method. The source voltage of the input and output protection circuits, \( V_{DD0} \), is 3.3 V. The source voltage of the core circuit, \( V_{DD0} \), is 1.8 V. Test vectors are provided from a pattern generator. TTL compatible logic signals are generated from the generator, whose voltage is 5 V. In order for the signals from the generator to shift to 3.3 V signals, SSIs of 74HC00 are used in our experimental circuit. A resistor of 100 \( \Omega \) is used as the \( R_C \). \( V_{RC} \) is measured with a digital oscilloscope. A soft open defect is inserted by adding a resistor, \( R_f \), to \( S1 \). A hard open defect is inserted by eliminating the interconnect of \( S1 \) in the defect-free PCB circuit.

Figure 13 shows the waveforms of \( V_{RC} \) in a defect-free circuit and in defective ones. These were obtained by providing the test vectors in Fig. 3 per 1 \( \mu \)sec. As shown in Fig. 13, both soft open and hard defects are detected by our test method. It is seen that there are some differences between the measured waveforms and the ones derived by the SPICE simulation. These stem from differences in the parasitic capacitances and resistances between the simulation circuit and the PCB circuit. However, since the quiescent \( V_{RC} \) values of \( S1 = H \) in the defective circuits are smaller than in the defect-free circuit, they are detected by our test method. Also, the defective TSV will be located by examining which interconnect a high-level signal is provided to.

Waveforms of \( V_{RC} \) with test vectors provided per 100 nsec and 50 nsec are shown in Fig. 14 and Fig. 15, respectively. High frequency components appear in waveforms of \( V_{RC} \) as shown in the figures. It reveals that it is difficult to measure quiescent \( V_{RC} \) values when tested at high speed.
However, $V_{RC}$ values that appear after dynamic changes of $V_{RC}$ caused by the application of $S1 = H$ are smaller than those of the defect-free circuit in Fig. 14(c). Thus, the soft open defect is detected by our test method just as in the cases of the hard open defects. For the soft open defects, $R_f = 1 \, \text{k}\Omega$.

Since the appearance time of the quiescent $V_{RC}$ is reduced when each test vector is provided per 50 nsec as shown in Fig. 15, it seems that the open defects are not detected by our test method.

3.3 Estimation of test speed

Our test method is based on the quiescent $V_{RC}$. Thus, the speed of our test method depends on the appearance time of the dynamic $V_{RC}$ that is defined as the time from test input vector application to the disappearance of dynamic change in $V_{RC}$. The appearance time can change due to parasitic capacitance and the resistance of the interconnects between dies and between the TST terminal and the $V_{RC}$ measurement circuit. Thus, it is impossible to estimate the maximum test speed of our test method from our SPICE simulation results and the experimental results of our PCB circuit.

However, parasitic capacitance and resistance between dies are smaller than those between our prototype IC and a PCB. Thus, interconnects can be tested at a higher speed in 3D IC tests than in our PCB circuit tests. We think that the open defects in a 3D IC are detected by our test method at a test speed of at least 10 MHz.

4. Conclusion

We propose an electrical test method and a testable design method for detecting and locating open defects at interconnects between dies inside a 3D IC. Also, we examined the feasibility of the testing using a SPICE simulation. The results reveal that hard open defects and a resistive open defect of 100 $\Omega$ occurring at an interconnect between two dies can be detected at a test speed of 1 GHz by the test method. Furthermore, we have examined whether such open defects in a PCB circuit made of our prototype IC which is designed using our testable design method can be detected by our test method. The results show that open defects at interconnects between dies in a 3D IC can be detected at a test speed of at least 10 MHz.

3D ICs made of TSVs, each of which has only two terminals connected, are targeted in our test method. There can be 3D ICs made of TSVs, each of which has more than two terminals connected. Thus, it is a future project to develop a test method and a testable design for the 3D ICs.

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References


