Fine Pitch Wirebonds on Ultra Low-k Device


*Yamato Laboratory, IBM Japan, Ltd., 1623-14 Shimo-tsuruma, Yamato, Kanagawa 242-8502, Japan
**IBM Research – Tokyo, IBM Japan, Ltd., 1623-14 Shimo-tsuruma, Yamato, Kanagawa 242-8502, Japan
***IBM Systems and Technology Group, 1000 River Street, Essex Junction, Vermont 05452-4299, U.S.A.
****IBM Systems and Technology Group, 2070 Route 52, Hopewell Junction, New York 12533-6683, U.S.A.
*****IBM T.J. Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, New York 10598, U.S.A.

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Abstract

The mechanical integrity of wirebonds are sensitive to structures under the bond pads of ultra low-k dielectric devices. The authors studied the mechanical performance of wirebonds on 32-nm test chips with various layouts of lines and vias under the 35-µm-pitch bond pads, various stacks of dielectric layers, and a range of bonding process conditions. Poor mechanical integrity resulted in the pad tearout failure mode at wire pull testing. The thickness of the SiO₂/FTEOS layer and the density of the vias in the ULK layer are the key factors for good wirebond integrity, manufacturability, and module-level reliability with ultrafine pitch wirebonds. The wirebond experimental results were analyzed by capillary indentation, excessive bond force parameter and finite element method (FEM). The authors found that only excessive bond force does not increase the rate of pad tearout and 2D FEM model can correlate the location of pad tearout in the ULK layers with calculated highest stress point which occurs by the ultrasonic vibration during wirebonding process.

Keywords: Chip Package Interaction, Wirebonding, Low-k Dielectric, Wire Pull Testing, Mechanical Integrity

1. Introduction

As semiconductors shrink, the resistive-capacitive (RC) delay in the back-end-of-line (BEOL) wiring layers is becoming one of the greatest technical challenges to improving the performance as the scale shrinks. Two main approaches have been tried to reduce RC delays. One is replacement of Al wires with Cu, which has lower resistance. The other is low-k and ultralow-k (ULK) interlayer dielectric (ILD) materials that reduce the parasitic capacitance. Low-k and ultra low-k ILD materials are generally more fragile than conventional ILD materials such as SiO₂ or fluorinated tetraethyl orthosilicate (FTEOS). As the mechanical properties of the ILD become worse, co-development of the chip and package, the chip package interactions (CPI) becomes more important for robust mechanical integrity in the wafer and assembly processes.

CPI includes ILD damage, cracks, and delamination due such factors as mismatches in the coefficients of thermal expansion (CTE) between the silicon chips and molding or underfill resins, CTE mismatches between chips and organic chip carriers, mechanical and thermal effects on the chip edges during dicing, and mechanical affects of wirebonding. Development efforts have focused on CPI for low-k and ultralow-k devices. IBM has released CPI evaluations for 90-nm,[1] 65-nm,[2] and 45-nm[2, 3] devices. Pad tearout often occurs during wirebonding and in the wire pulling test.[4, 5]

We studied the mechanical integrity of 32-nm test die[6] with a 35-µm ultrafine bond pad pitch. We measured the frequency of pad tearouts for various ILD stacks and structures under the bond pads, including analysis of pad tearouts through experiments and finite element analysis.

2. Wire Pull Testing and Pad Tearouts

A wirebond is a chip-to-package interconnection using Au, Cu, or Al wire. Our work focused on Au wires because there was no commercially available thin Cu wire which is suitable for 35-µm bond pad pitch. Also Al wire is normally used for wedge bonding with wider pad pitches. Ball bonding is the interesting part of the wirebonding since it is
done on the chip terminal pads. The key factors that affect
the mechanical integrity under the bond pads are (1) the
force of the impact of the initial ball contact against the
bond pad, and (2) the compression and ultrasonic power of
the thermosonic bonding phase.

A wire pull test is a standard method to assess wirebond
integrity. A pull test is done by hooking the wire loops, as
shown in Fig. 1. The normal break mode is the wire neck
break shown in Fig. 2(a). The wire neck is the weakest
part of the loop since the wire neck is softer than the other
area of wire because of a larger grain structure. The larger
grain structure is formed by the heat of an electrical spark
to create the initial free air ball. The pad tearout mode in
Fig. 2(b) is the break mode of our concern, in which the
bonded ball comes off along with Al bond pad and the
underlayer dielectric films. Such failures show poor
mechanical integrity, which can cause manufacturing and
reliability problems.

3. Sample Description

The features of our test samples appear in Table 1.

We prepared three different BEOL stacks as shown in
Fig. 3. The 5-2-2 stack means there are five 1x (minimum
line and space design rule) layers in the low-k at the bot-
tom wiring layer and in the ULK at the four upper wiring
layers, two 2x (approx. 2 times the line and spaces of the
minimum design rule) layers in the ULK, and two 8x
(approx. 8 times the minimum rules) in the FTEOS. A
very thin dielectric cap layer is applied on top of each wir-
ing layer. The Cu dual damascene process is used in the

<table>
<thead>
<tr>
<th>Table 1 Features of test vehicles.</th>
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</thead>
<tbody>
<tr>
<td>Chip technology</td>
</tr>
<tr>
<td>Chip size</td>
</tr>
<tr>
<td>ILD material</td>
</tr>
<tr>
<td>BEOL stack</td>
</tr>
<tr>
<td>Structures under pads</td>
</tr>
<tr>
<td>Pad pitch</td>
</tr>
<tr>
<td>Pad opening</td>
</tr>
<tr>
<td>Pad metallurgy</td>
</tr>
<tr>
<td>Pad thickness</td>
</tr>
<tr>
<td>Wire material</td>
</tr>
<tr>
<td>Wire diameter</td>
</tr>
<tr>
<td>Probe mark</td>
</tr>
<tr>
<td>Package type</td>
</tr>
</tbody>
</table>

BEOL stack.

Table 2 shows typical material properties of the ILD film
materials. These values are from the FEM analysis
described below.

We tested three different wire/via designs under the
bond pads on the test chips. Figure 4 shows the structures
under the bond pads. Type A is a serpentine structure that
contains wiring lines under the bonding area without any
via connections. Type B is a chain that goes up and down
in the ILD layers with via stack structures inserted
between adjacent daisy chains. Type B has via connections
under the bonding area with variations in the wiring and
via density. Type C is a via stack design with metal squares
in the wiring level. The via stack structures are isolated
from each other. Type C has the highest average via den-
sity (count per unit area) of the tested underpad struc-
tures.
4. Experiments and Results

4.1 Wirebond Experiment

A bond parameter matrix was used for the wirebond experiment. Three key parameters were picked as experimental variables: bond time, bond force, and ultrasonic power. Before defining the parameters, preliminary bonding trials were used to define the feasible parameter range for which there is no pad attachment failures during the ball bonding and no balls larger than the 29-µm pad openings. For the initial free air ball size and initial ball contact conditions, one condition was held constant and used for each experimental matrix. The initial free air ball size was optimized so that the largest balls would fit in the pad openings based on standard manufacturability criteria,[7] and the initial ball contact conditions were carefully optimized for the small balls without damage to the structures under the bond pads.

The defined bond parameter matrix was used for 3 different BEOL stacks. Wire pull tests were performed for each type of structure under the pad with each BEOL stack. Figure 5 is the results of pad tearouts against BEOL stacks and the structures under the pads. The pad tearout number is the total for all of the bond parameter legs. This data indicates the pad tearouts strongly depend on the BEOL stacks and the structures under the pads.

Figure 6 is a plot of pad tearouts against the average via density. Only the 5-2-1 stack was evaluated with various via densities and a single bond parameter set. The Type C structure has the highest number of vias among the tested structures, so it is labeled as 100% relative via density. Type B has 3 different via chain pitches, and the relative via density was calculated for each pitch. Type A does not have vias, so this is 0% relative via density. According to this plot, 0% via structure has a small percentage of pad tearouts, and low relative via density drastically increases percentage of pad tearout. As relative via density increases up to 40%, the pad tearout rate decreases. Although there is no data at 50% relative via density, the data suggests there would be almost no pad tearouts at that density. This indicates that the higher density of Cu lines and via structures can strengthen the mechanical integrity under the bond pads, but less than 40% relative via density weakens the integrity for the bonding conditions used in this experiment.

Figure 7 is a scanning electron microscope (SEM) photo
of a pad tearout with a 5-2-1 BEOL stack. The pad tearout region was sectioned with a focused ion beam (FIB) and a SEM photograph was taken. The photograph shows the separation occurred in the 2x ULK layer.

These results show:

a) 5-2-2 resisted pad tearout and demonstrated good wirebond manufacturability. 5-0-1 is better than 5-2-1. Different ULK-layer stacks have different pad tearout rates. Comparing 5-2-1 and 5-2-2, the FTEOS thickness dominates in preventing pad tearouts.

b) Low relative via density (< 40%) under the bond pad seems to disrupt the mechanical integrity. No vias at all is much better than a low via density.

c) Fractures are likely in the 2x ULK layer for the 5-2-1 stack and 1x ULK layer for the 5-0-1 stack.

### 4.2 Module Reliability Tests

Module level reliability stress tests are performed after packaging the 5-2-2 test chip into a 37.5-mm² plastic ball grid array (PBGA). The stress samples are preconditioned (JEDEC Level-3) before the stressing begins. The samples pass the JEDEC standard stress tests, as shown in Table 3. We obtain similar result of 5-0-1 test chip without fail, but 5-2-1 test chip has a fail with a specific structure under the pad.

#### 5. Analysis of Bond Force and Ultrasonic Vibration

Although 5-2-2 stacks give us good results in the wire pull test and module reliability tests, 5-0-1 and 5-2-1 have pad tearouts with specific structures under the pad. The significant difference between 5-2-2 and 5-0-1/5-2-1 is the thickness of FTEOS over the ULK layers. The two 8x FTEOS layers act as a mechanical barrier, but one 8x FTEOS layer is not as good. We also tried to understand how the stress in ULK is generated and distributed in the bonding sequences and to see if it conforms to the results described in the previous section.

#### 5.1 Indentation by Capillary

The test chip prepared here has different stacks from the previous test chip. The stack is three 1x Low-k at the bottom, three 2x ULK layers in the middle, and FTEOS on top. This chip uses 40-µm-pitch bond pads as this is the minimum pad pitch with via chain structure on this test chip. Indentation was done with a capillary using a wire bonder on the bond pads above the stacked via chains. Four different indentation loading forces were applied to the bond pads. We tested the electrical resistance before and after the indentations. Table 4 shows the electrical test results for the stacked via chains. As the loading force increases, the open failure rate also increases. Some of the open samples were sectioned with FIB and observed with the TEM. Figure 8 is a TEM photograph that shows the cracks are located near the bottom of the via in the ULK layers.

<table>
<thead>
<tr>
<th>Loading force of indentation (N)</th>
<th>Opens / Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.98</td>
<td>2 / 6</td>
</tr>
<tr>
<td>0.49</td>
<td>3 / 9</td>
</tr>
<tr>
<td>0.25</td>
<td>2 / 8</td>
</tr>
<tr>
<td>0.10</td>
<td>0 / 12</td>
</tr>
</tbody>
</table>

**Table 3** Module reliability test results of 5-2-2 test chip.

<table>
<thead>
<tr>
<th>Stress item</th>
<th>Condition</th>
<th>Duration</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal cycle</td>
<td>-55/125°C</td>
<td>1000 cycles</td>
<td>Pass</td>
</tr>
<tr>
<td>High temp. storage</td>
<td>150°C</td>
<td>1000 hours</td>
<td>Pass</td>
</tr>
<tr>
<td>Temp. humidity bias</td>
<td>85°C, 85% RH</td>
<td>3.7 V, 1000 hours</td>
<td>Pass</td>
</tr>
</tbody>
</table>

(n = 90 for TC, n = 60 for HTS and THB)
5.2 Effect of Excessive Bond Force

To investigate how the bond force influences the pad tearouts, we tested the application of excessive bond force before the normal bonding. The test used a 5-2-1 stack chip like that used in the wirebond experiment. In this experiment, excessive force was applied in advance without boning the balls before the normal bonding procedure. There was also a control sample.

- Sample E\textsubscript{f}: Excessive bond force (0.24 N) without ultrasonic power.
- Sample E\textsubscript{c}: Control sample without pre-bond force.

This is a normal bonding sample.

Both samples were bonded using the standard bonding conditions. The only difference was that sample E\textsubscript{f} received the high force pretreatment. Although cracks are observed with 0.25 N indentations from the capillary, there are no significant differences in the pad tearout rates between the E\textsubscript{f} and E\textsubscript{c} samples. This implies that there is no damage in the ILD when the excessive force is applied through the Au balls because Au ball is much softer than the capillary. The pre-bonding force is more than 2.5 times higher than the normal bonding force for 35-\mu m-pitch bond pads, so it is clear that the bond force used for this fine pitch does not affect the ILD integrity during the wirebonding.

5.3 FEM Analysis

Figure 10 shows the ball bonding model consists of the Au wires and balls, Al pads, ILD, Cu wires and via, and the capillary. The material properties of the ILD are shown in Table 2 and material properties of the metal conductors appear in Table 5. The capillary is assumed to be a rigid body in this model. The capillary and the gold are not connected, but have constant static friction at the contact interface. The wirebond is typically processed at 175°C for PBGA, but the temperature effects are ignored here. Dimensions such as ball size, pad opening and ILD thickness in this model were defined based on the test chip design. The various via stack structures were modeled under the bond pads. All the analyses were performed with 2D models.

There were 6 steps including analysis:

- Step 1: The capillary pushes the free air balls against the Al pad by 10 \mu m from the initial contact. Au ball is not connected to the Al pad during this step. This is a contact analysis with static friction between the Au balls and the Al pads. The Au ball is strongly deformed this step.
- Step 2: The bonded balls and Al pads are connected.

In this step the capillary displaces the Au wires and balls by 2 \mu m to the right.

- Step 3: The capillary displaces the balls by 4 \mu m to the left.
- Step 4: The capillary returns to the original point. Steps 2 through 4 are simulating one cycle of the back and forth movement of ultrasonic treatment.
- Step 5: The capillary is released.
- Step 6: The wires are pulled for the wire pull test.

The stresses in the ILD layers under the ball bonding area were examined after each step. This pre-bonding force does not affect the integrity of the ILD. The most interesting part is Step 2 through Step 4, which simulates ultrasonic motion. Figure 10 shows a 5-2-1 stack at Step 3. As the capillary pushes the wire neck to the left, the highest tensile stress occurs on the right side under the ball. In the ILD layers, the highest point is located at the 2x ULK layer which matches the result of the cross-section of the pad tearout. Figure 11 compares the primary principal stress of three different BEOL stacks. The maximum stress in this analysis is tensile stress.

The analysis shown in Fig. 12 is three different via densities for 5-2-1 stacks. The middle density is the base model used for the stack comparisons from Fig. 11. The induced stresses were studied after running Steps 1 to 6 at the three different via densities. Figure 13 compares the maximum

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### Table 5 Material properties of metal conductors.

<table>
<thead>
<tr>
<th></th>
<th>Au wire/ball</th>
<th>Al pad</th>
<th>Cu wire/via</th>
</tr>
</thead>
<tbody>
<tr>
<td>Elastic modulus  (GPa)</td>
<td>78</td>
<td>48</td>
<td>110</td>
</tr>
<tr>
<td>Poisson’s ratio</td>
<td>0.33</td>
<td>0.33</td>
<td>0.33</td>
</tr>
<tr>
<td>Yield stress (MPa)</td>
<td>85</td>
<td>30</td>
<td>290</td>
</tr>
<tr>
<td>Tangent modulus (MPa)</td>
<td>1.2</td>
<td>1.2</td>
<td>1.2</td>
</tr>
</tbody>
</table>
stress in the ILD layers at Step 3. The highest stress points are close to the location shown in Fig. 10.

The stress induced by the wire pull in Step 6 was also studied. The FEM analysis results do not show clear differences among the three BEOL stacks.

Although the 2D model does not precisely represent the design of the structures under the pad used for these experiments, the first principal stress data obtained from Step 3 traces the data trend of the pad tearout rates as shown in Fig. 6. It is still difficult to quantitatively correlate the calculated stress and pad tearout rates. This analysis is based on a static model, but ultrasonic bonding is a dynamic process. To understand in more detail the ultrasonic mechanisms in the ILD layers and the stress induced by wire pull test, analysis with dynamic 3D models is called for. We believe that the wire pull test does not characterize the initial crack propagation because the wire pull test finds the peak strength, which should be the fracture strength of the thick oxide layers. The development of a measuring system to characterize the initial crack propagation is needed to better understand the fracture mechanisms in the ILD layers.

6. Summary

We found that the 32-nm chip with 5-2-2 BEOL stacks has good wirebond mechanical integrity and good reliability for PBGA. Our experimental data indicates the FTEOS thickness is a key factor to prevent pad tearouts. The via density in the ULK layer is another key factor that affects pad tearouts. Using high-density vias actually increases the integrity in the ULK layers, and density below 40% relative to the maximum via density increases the pad tearouts. As the via density decreases, the pad tearouts increase. However 0% via density is much better than low density vias. Our analysis indicates that the only bond force that is applicable at very fine pitches does not have a significant impact in the ULK layer. The 2D FEM analysis shows good correlations between the highest principal stress points and the fractured layers of the pad tearouts. Understanding the detailed fracture mechanism for the initial crack propagation in the ULK layer is our next challenge to integrate the next generation ULK.

Acknowledgment

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References


