Multi-Chip Module Fabricated by W-CSP Method using Excimer Laser Via-Hole Formation and Cu Plating


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Abstract
Recently high-density packaging technologies have been in strong demand in an effort to realize the ubiquitous networking society. A wafer-level chip size packaging (W-CSP) technology is one of the most promising technologies for high density and environmentally-friendly packaging. The purpose of this study is to propose a fabrication method for a multi-chip module system using W-CSP technology. In this study, we fabricated a two-chip module with W-CSP using an excimer laser to form via-holes and electro-plating to fill the via-holes. This study has two main new technologies: one is new via-hole formation using an excimer laser that makes small (30 μm diameter) and deep (50 and 100 μm) via-holes, with a micro-lens array used to shorten via-hole formation time. The second new technology is new copper electroplating techniques to fill the via-holes which have same diameter (30 μm) and different depths (50 and 100 μm) by controlling additives and agitating conditions. In this study, we fabricated a two-chip module, and both chips were covered by resin simultaneously. The second chip, whose thickness was 50 μm, was mounted on a wafer (first chip) after the first chip had completed the wafer process. The second chip was thinned and mounted by die attachment film (DAF). Next, the mounted chips were spin-coater with polyimide or epoxy resin about 100 μm in thickness. Two types of via-hole with different depths, 50 and 100 μm, were formed by excimer laser to connect the wafer and mounted chip pads. Both types of via-hole had a diameter of about 30 μm. After via-hole formation, seed layers, sputtered Ti and Cu films, are necessary for subsequent copper electro-deposition. Using microscopy measurement, the seed layers were seen to be uniformly formed from the top to the bottom of the via-hole. Using a general mixture of additives, brightener, leveler, and suppressor, the via-holes were completely filled. By controlling the suppressor effect, the 100 μm deep via-holes were perfectly filled with the copper electroplating. Both mechanical agitation and current density are effective to ensure via-hole filling and optimization of these two factors is very important in filling via-holes. Moreover, an additional electroless copper seed layer to increase conductivity near the bottom of the via-hole is also effective to suppress voids there. Finally, the conductivities between the first and second chips were confirmed for the multi-chip module fabricated using W-CSP with excimer laser and copper electro-plating.

Keywords: Multi-Chip Module, W-CSP, Excimer Laser, Cu Plating, Via-hole Filling

1. Introduction
In today’s networking society, there is a strong push to make electronic devices smaller and multi-functional, so that they will be handy and wearable. Semiconductor technologies have been the main means of realizing this ubiquitous networking society, but now it is becoming seriously difficult to miniaturize semiconductors at a lower cost, because finer processes increase costs significantly.

In addition, physical limitations, such as the thickness of gate oxide films, are being reached. To address this situation, many researchers have actively investigated the system-in-package (SiP) concept, referring to a single package containing many chips that represents a complete system.

Three-dimensional (3D) packaging technology is of great importance in this development. Several kinds of 3D
packages such as wafer-to-wafer bonding technologies[1] have been applied to things such as image sensor chips[2] and shared memory.[3] A chip-to-wafer technology has also been actively investigated.[4] This paper reports on a SiP (chip-to-wafer) that was fabricated using wafer-level chip-size package (W-CSP) technologies. With this method, new chips are bonded on the wafer after it has been through a wafer manufacturing process (front-end and back-end processes). A resin such as polyimide is coated onto the chip and wafer, and via-holes are opened by an excimer laser combined with a micro-lens array. Finally the via-holes are filled by copper electro-plating.

One of the features of this method is the combination of excimer laser and micro-lens array, which shortens the time needed to form the via-holes. There are two types of via-holes: those that connect bonded chips are 50 μm deep and those that connect wafers have depths of 100 μm. Another feature is the electro-plating technology used to simultaneously fill via-holes of different depths.[5] Filling via-holes with high-aspect ratios has been actively investigated for through silicon vias (TSV),[6, 7] but few for W-CSP.[8] In this paper, we investigated three new technologies: the first is a trepaling technology that changes the taper of via-holes; the second is the reinforcement of the seed layer by electroless Cu plating; and the third is via-hole filling method without voids. Moreover, we propose a via-hole filling mechanism for via-holes with high aspect ratios. Finally, the conductivities between the first and second chips are confirmed and the measurements indicate good via-hole filling results.

2. Experimental

In this study, TEG chips (Phase0, Hitachi High-Technologies Co., LTD.) were used as the mounted chips; they were thinned to 50 μm thickness and attached to the wafer with DAF tape. The pad pitch of the TEG chip was 130 μm. The polyimide resin was applied, and via-holes were formed by a MMLD (micro multi laser driller, Phoeton Corp.) which includes the micro-lens array. Both titanium and copper were sputtered, and electro-plating was performed to fill the via-holes and wiring on the surface of the polyimide. The experimental methods are almost the same as those of the previous report.[5]

Figure 1 presents the cross-sectional schematic models of the multi-chip module investigated in this study.[5] Two chips are contained in a chip-size package formed by the W-CSP method. Copper filling of via-holes with different depths is a necessary part of this method. Figure 2 demonstrates the typical process used in this study.[5] The MMLD combined eximer laser and micro-lens array was used in this study.[5] The combination made it possible to form many via-holes at once. This method is effective to shorten via-hole formation time and to increase throughput.

In this study, we used electroless Cu plating to reinforce the seed layers. Before electroless Cu plating, cleaner (C3320, Rohm and Hass Co. Ltd.), predip (CAT404, Rohm and Hass Co. Ltd.) and catalyst (CAT404 and CAT44,
Rohm and Hass Co. Ltd.) were used to prepare the surface conditions and to start electroless plating. Copper wiring was electroplated using cup-type plating equipment (EEJA Co. Ltd.).

Resistivity was measured using a combination of manual prober and digital multimeter (2502A, Yologawa Electric Co. Ltd.).

3. Results and Discussion
3.1 Mounting the second chips on the first chips

Figure 3 shows photographs of the mounted, second, chips on the first chips, or wafer. The 408 second chips were mounted on the 8-inch wafer by a mounter.

3.2 Via-hole formation by MMLD

Figure 4 shows the surface view of a via-hole after excimer laser irradiation. As shown in Fig. 4, the via-holes with different depths, on the first or second chip, are clearly observed.

3.3 Film formation inside via-hole by sputtering

As reported in a previous paper,[5] the seed layers were formed by sputtering, titanium to 0.15 μm thickness and copper to 0.3 μm, for a total thickness of 0.45 μm. However, the thickness of the sputtered film reported in the previous paper was 10 nm on the side walls and 20 nm at the bottom of the via-hole.[5] As mentioned above, the sputtered layer was 450 nm thick, so on the side walls and the bottom the layers were relatively thin, but the sputtered films were continuously formed.

3.4 Via-hole filling by plating method

As mentioned above, the seed layers are very thin on the side and bottom of via-hole. From the viewpoint of mass-production, overly thin seed layers lower the packaging yield due to incomplete via-hole filling. Next we attempted reinforcement of seed layer by electroless copper plating.

Figure 5 shows a cross-sectional micrograph of a via-hole after reinforcement of the seed layer by electroless Cu plating. The copper thickness on the surface area is 4.83 μm.

Figure 6 illustrates the expansion of the cross-sectional micrograph after reinforcement of the seed layer by electroless Cu plating. The copper on the bottom of the via-hole is 2.23, μm thick. The thickness deference between the surface film and that at the bottom area is significantly decreased, down to a factor of two. Before the reinforcement of the seed layer by electroless Cu plating, the difference is more than twenty times. Moreover, as shown in Fig. 6, the copper thickness of the side walls is the same as that on the bottom of the via-hole. These results were...
achieved by the intrinsic advantages of electroless plating, i.e., uniform plating.

For practical production, the thickness of the seed layer should be thinner to increase throughput, and as was confirmed in this study, it is possible at less than half of the above values, i.e., about 1 μm.

3.5 Mechanism of via-hole filling

Based on this investigation, both agitation and current density are very important for via-hole filling. Agitation makes the suppressor more effective. Figure 7 demonstrates the effect of agitation and current density on via-hole filling, respectively. As shown in the left figure, the plating film thickness increased with increasing current density, however the corners of the via-holes were preferentially plated. This preferential deposit makes voids in the via-holes. On the other hand, the plating was suppressed with increasing agitation speed. Since higher agitation speed make the role of suppressor more effective, the plating is suppressed both on the surface and inside the via-holes at the highest agitation speed, 50 rpm.

Based on the above results, via-hole filling should be done under relatively high suppressing conditions to eliminate void formation in the via-holes. At a minimum, the plating on the corners of via-holes should be suppressed. Since the agitation effect is highest on the surface and lowest at the bottom of via-hole, the control of agitation, suppression, and current density are important.

Next, we investigated the high-agitation region for high-plating suppression of via-hole corners. This higher-agitation region allows a higher current density, because the corners of via-holes are highly suppressed and this suppression makes void-free via-hole filling.

Figure 8 shows the results of via-hole filling with high agitation and high current density. As shown in Fig. 7, the higher agitating conditions suppress plating and the higher current density is necessary for via-hole filling. In this study, the Cu electroplating time was set at 4.5 hours.
From the results shown in Fig. 8, the optimum conditions are near an agitation speed of 70 rpm and current density of 1 A/dm$^2$.

Further investigation of the near optimum conditions showed complete via-hole filling as shown in Fig. 9. Figure 9 shows a cross-sectional micrograph of a via-hole plated under the optimum conditions. No void was observed. Therefore this via-hole filling method is effective for fine via-holes with high aspect ratios.

Figure 10 demonstrates different taper angles and their effect on via-hole filling. There are two main methods to change the taper angle: one is the common method of changing the mask size, laser power, pulse number and work distance; the other method is the trepanning method that is shown in Fig. 10a. In the trepanning method, the laser beam is rotated with a changing diameter, 50 μm to 30 μm. This trepanning method is effective to eliminate residual substances at the bottom of the via-hole. As mentioned above, the taper angle is one of the most important factors in seed layer formation using the sputtering method. Figure 10 shows cross-sectional SEM micrographs of the samples with different taper angles, which were plated at once. Therefore the via-holes with high
taper angle are difficult to fill completely, because their volumes are larger than those with a lower taper angle. The results of Fig. 10 coincided with the forecast mentioned above. There is no void for all samples.

Figure 11 shows cross-sectional SEM micrographs of the sample fabricated in this study. Both 50 μm and 100 μm depth via-holes have been filled.

Figure 12 shows a photograph of a multi-chip package fabricated with the W-CSP method investigated in this study. Figure 12a shows the second chip area. The via-holes to the second chip can be recognized by comparing Fig. 12b. The copper wiring was formed to connect the first and second chips. Table 1 shows the numbers of via-holes and wiring lengths for the combination of pads.

Figure 13 shows a schematic model of the conductivity test, the arrangement of testing chips. The A chip is located on the left, the B chip is in the center and the C chip is on the right.

Figure 14 shows a schematic model of the conductivity test, the arrangement of testing pads. Table 2 summarizes the results of the conductivity measured between pads as shown in Fig. 12. The difference in measuring the terminal points is a difference of wiring length, and the resistivities of each point are different. However, at the same measuring terminal, the resistivity values of different point chips were almost the same. These results show the high uniformity of this process and the via-hole filling.

Figure 15 shows the electroplated copper posts which were formed at the top, center, bottom, left and right positions of an 8-inch wafer. The variation of post size is less

<table>
<thead>
<tr>
<th>Terminal Point</th>
<th>Number</th>
<th>Wiring distance (mm)</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>50 μm depth</td>
<td>100 μm depth</td>
</tr>
<tr>
<td>1 –1'</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>2 –2'</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>3 –3'</td>
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<tr>
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<td>0</td>
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<td>22</td>
<td>6</td>
</tr>
<tr>
<td>4 –1</td>
<td>59</td>
<td>20</td>
</tr>
</tbody>
</table>

Fig. 13 Schematic model of conductivity test: arrangement of testing chips.
Fig. 14 Schematic model of wiring of the sample fabricated in this study.
than 3%. This value shows the high uniformity of this electroplating.

4. Conclusion

Via-hole formation using MMLD and filling using electro-plating were investigated and the following results were obtained.

(1) A micro-lens array was designed to shorten the via-hole formation time. After via-hole formation, a seed layer of sputtered Ti and Cu films was necessary, followed by copper electro-deposition.

(2) Via-holes with 30 μm diameter and 100 μm depth were perfectly filled by copper electro-plating. Therefore this study has shown it is possible to form a multi-chip module using W-CSP techniques with an excimer laser.

(3) For practical production, higher uniformity of the seed layer is necessary as well as reinforcement of the seed layer by electroless Cu plating. The thickness difference between the surface and bottom area decreased to a factor of two. Before the reinforcement of the seed layer by electroless Cu plating, the difference was more than twenty times.

(4) To achieve void-free via-hole filling, a high-agitation condition is necessary in order to suppress plating on the corners of the via-holes. The high-agitation conditions made the role of suppressor more effective.

(5) Under high-agitation conditions, a higher current density was allowed.

(6) Controlling both agitation and current density was key to filling the via-holes with high-aspect ratios completely.

(7) In this study, the multi-chip module was fabricated using the W-CSP method combined with an excimer laser and plating method.

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References


