Abstract

A multi-chip module (MCM) was fabricated using an excimer laser driller and electro-plating. This method contributes to the interconnection properties of the MCM. First, a second chip with a thickness of 50 \( \mu \text{m} \) was mounted on a wafer that had been created by a wafer process, and polyimide with a thickness of about 100 \( \mu \text{m} \) was applied by a spin-coater to cover the mounted chips. Two types of via-holes, with depths of 50 and 100 \( \mu \text{m} \), were formed by the excimer laser to connect the wafer and mounted chip pads. The excimer laser driller with a micro-lens array formed two types of via with diameters of about 30 \( \mu \text{m} \) simultaneously. Damage caused by the excimer laser irradiation was examined by direct laser irradiation of the FET transistor gate. Properties of the FET transistor did not change even after 500 pulses of 400 mJ/cm\(^2\) which is sufficient for via-hole formation. A micro-lens array was designed to shorten the via-hole formation time.

After via-hole formation, a seed-layer of sputtered Ti and Cu films were necessary, followed by copper electro-deposition. Microscopy measurements confirmed that the seed-layers were uniformly formed from top to bottom of the via-hole. Generally the mixture of additives to complete the via-hole filling consists of brightener, leveler, and a suppressor. By controlling the leveler concentration, a via-hole with a diameter of 30 \( \mu \text{m} \) and a depth of 100 \( \mu \text{m} \) was perfectly filled by copper electroplating. In this way the multi-chip module was created by wafer-level chip size technologies (W-CSP) using an excimer laser driller.

Keywords: W-CSP, Excimer Laser, Micro-Lens Array, Electro-Plating

1. Introduction

In today's networking society; there is a strong trend to make all electronic devices smaller and multi-functional, so that they will be handy and wearable. Semiconductor technologies have been the main support in realizing this ubiquitous networking society, but now it is becoming seriously difficult to miniaturize semiconductors at a lower cost, because finer processes make costs much higher. In addition, physical limitations, such as gate oxide film thickness, are being reached. To address this situation, many researchers have actively investigated the system in package (SiP) concept, referring to a single package containing many chips that represents a complete system.

The three dimensional (3D) packaging technology is great importance in this development. Several kinds of 3D packages such as wafer-to-wafer bonding technologies[1] have been applied to things such as image sensor chips[2] and shared memory.[3] A chip-to-wafer technology has also been actively investigated.[4] This paper reports on SiP (chip-to-wafer) that has been fabricated using wafer-level chip size package (W-CSP) technologies. With this method, new chips are bonded on the wafer after it has been through a wafer manufacturing process (front end process and back end process). A polyimide resin is coated onto the chip and wafer, and via-holes are opened by an excimer laser combined with a micro-lens array. Finally the via-holes are filled by copper electroplating. One of the features of this method is the combination of excimer laser and micro-lens array, which shortens the time needed to form the via-holes. There are two types of via-holes: those that connect bonded chips are 50 \( \mu \text{m} \) deep and those that connect wafers have depths of 100 \( \mu \text{m} \). Another feature is the electro-plating technology used to simultaneously fill via-holes of different depths.
2. Experimental

In this study, TEG chips (Phase0, Hitachi High-Technologies Co., LTD.) were used as the mounted chips; they were thinned to 50 μm thickness and attached on the wafer with DAF tape. The polyimide resin was coated and via-holes were formed by MMLD (micro multi laser driller, Phoeton Corp.) which consists of the micro-lens array. Both titanium and copper were sputtered, and electroplating was performed to fill the via-holes and wiring on the surface of the polyimide.

Figure 1 presents the cross-sectional schematic models of SiP investigated in this study. Two chips are contained in a chip size package by the W-CSP method. Copper filling of via-holes with different depths is a necessary part of this method. Figure 2 is a schematic model of an MMLD
combined eximer laser and micro-lens array. The combination made it possible to form many via-holes at once. Figure 3 shows test patterns and pad locations of the TEG chip. The pad pitch of the TEG chip was 130 μm.

3. Results and Discussion

3.1 Transistor damage from excimer laser irradiation

As shown in Fig. 1, the irradiation times required to form via-holes with different depths, 50 μm and 100 μm, are different. The irradiation time needed for shallower via-holes was much shorter than that for deeper ones, and the excimer laser continued irradiating until all via-holes were formed. The effects of excimer laser irradiation should be researched and irradiation conditions should be limited to the range within which there is no change to the transistor characteristics.

Figure 3 demonstrates the effect of laser irradiation on the relationship between gate voltage, Vg, and source-drain current, Id. The irradiated pad was directly connected to the gate electrodes. The transistor length/width, L/W, was 0.8/9.75 μm and the thickness of the gate insulator oxide film was 15nm. A voltage of 1V was applied between the source and drain. As seen in Fig. 4, no change of Vg-Id curves were observed when the pulse number was changed to 0, 1, 50, 250, 500 and 1,000, while pulse energy was kept at 500 mJ/cm².

3.2 Via-hole shape formed by MMLD

Figure 5 presents an overview of the via-holes, which were formed by 240 pulses with energy of 240 mJ/cm². Surface cleaning was performed by plasma ashing using CF₄ gas. Figures 6(a) and (b) are SEM micrographs of the PI film surface after excimer laser irradiation and after ashing. It is shown that ashing using CF₄ gas effectively...
cleaned the PI film surface after excimer laser irradiation.

3.3 Film formation inside via-hole by sputtering

Figures 7 and 8(a), (b) and (c) are cross-sectional views of via-holes after sputtering titanium to 0.15 μm thickness and copper to 0.3 μm.

A highly uniform sputtered film is necessary in order to proceed to via-hole filling. These figures confirm that sputtered film was formed from top to bottom of the via-hole. The top diameter of the via-hole was 50 μm and the bottom diameter was 30 μm.

From Figs. 7 and 8(a), (b) and (c), we can see that the thickness of the sputtered film was 10 nm on the side walls and 20 nm at the bottom of the via-hole. As mentioned above, the sputtered thickness was 450 nm, so the thickness on the side walls and the bottom were relatively thin, but the sputtered films were continuously formed.

Figure 9 is a cross-sectional SEM micrograph of the via-hole after it was filled with Cu plating formed by the excimer laser irradiation. The via-hole was completely filled by copper plating and the surface of the plated film was flat. Therefore, this method has high potential to produce high density via-holes with diameters less than 30 μm.

4. Conclusion

Via-hole formation by MMLD and filling using electroplating were investigated and the following results were obtained.

(1) Two types of via having different depths, 50 and 100 μm, were formed by the MMLD to connect pads between the wafer pad and mounted chip pad.
(2) The MMLD formed two types of via with a diameter of about 30 μm simultaneously.
(3) Damage from the excimer laser irradiation was examined by direct laser irradiation of the gate of the FET transistor. Properties of the FET transistor did not change even after 500 pulses of 400 mJ/cm², which was enough for via-hole formation.
(4) A micro-lens array was designed to shorten the via-hole formation time. After via-hole formation, a seed-layer of sputtered Ti and Cu films was necessary, followed by copper electro-deposition.
(5) Microscopy measurements confirmed the seed-layer was uniformly formed from top to bottom of the via-hole.
(6) Via-holes with a 30 μm diameter and 100 μm depth have been perfectly filled by copper electroplating. Therefore this study has shown it is possible to form a multi-chip module using W-CSP techniques with an excimer laser.

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References